

Deep Dive on **Kinetis E Series** **MCUs** with 5 V I/O and High EMC Performance

FTF-IND-F0471

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Agenda

- Kinetis E MCU Overview by Marketing
- Deep Dive of Key Features
- Real Case EMC Design Guideline
- Freedom and KE0x Peripheral Driver Lib
- Demo
- Summary



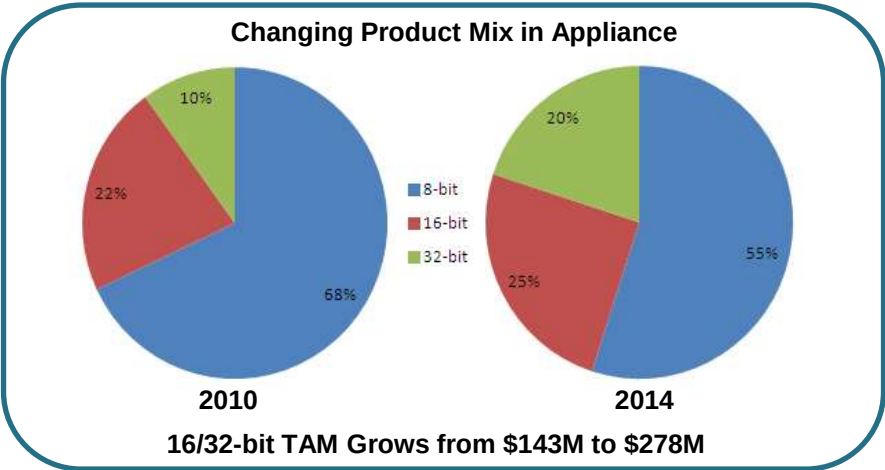
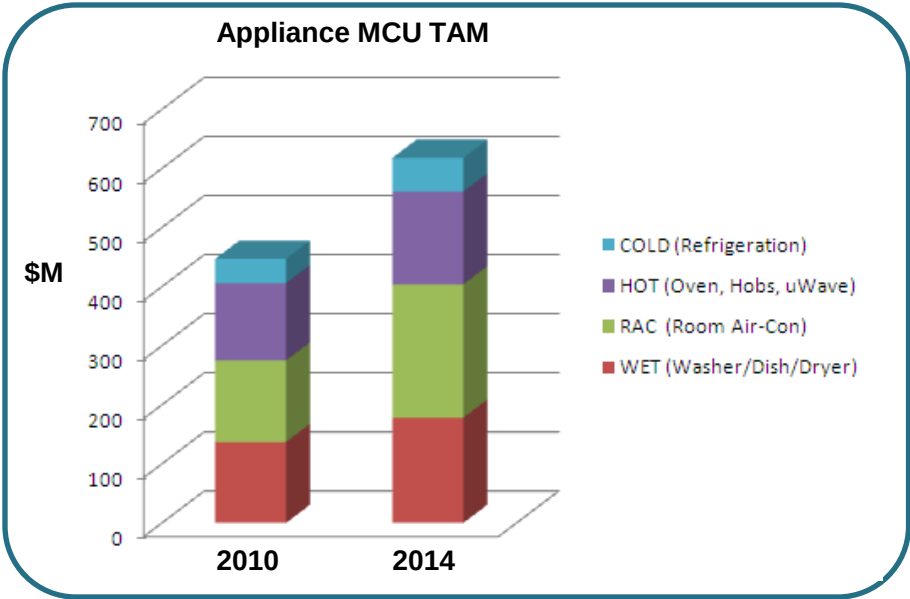
Kinetis E Overview

Market Needs 5V 32b KE

Key Segment – Appliances



Target Customers



Kinetis E

Strong Robustness

High Efficiency

Low Cost

Strong Robustness – EMC/ESD design technology ensure strong noise immunity performance

High Efficiency – Cortex-M0+ core up to 48MHz and 40x more than 8/16-bit MCUs

Low Cost – Optimized for cost-sensitive applications offering low pin count option

Kinetis E
First Tape
Out
Jan, 2013

Alpha
Customers
Engagement
May, 2013

Mar, 2013
First Sample

Aug, 2013
Mass
Production &
Product
Launch

Kinetis E-Series: Target Market

- Appliance
- DC fans
- Sewing Machine
- Elevator
- PLC
- Offline UPS
- Metering
- Breaker
- Surge Protection
- DC/DC



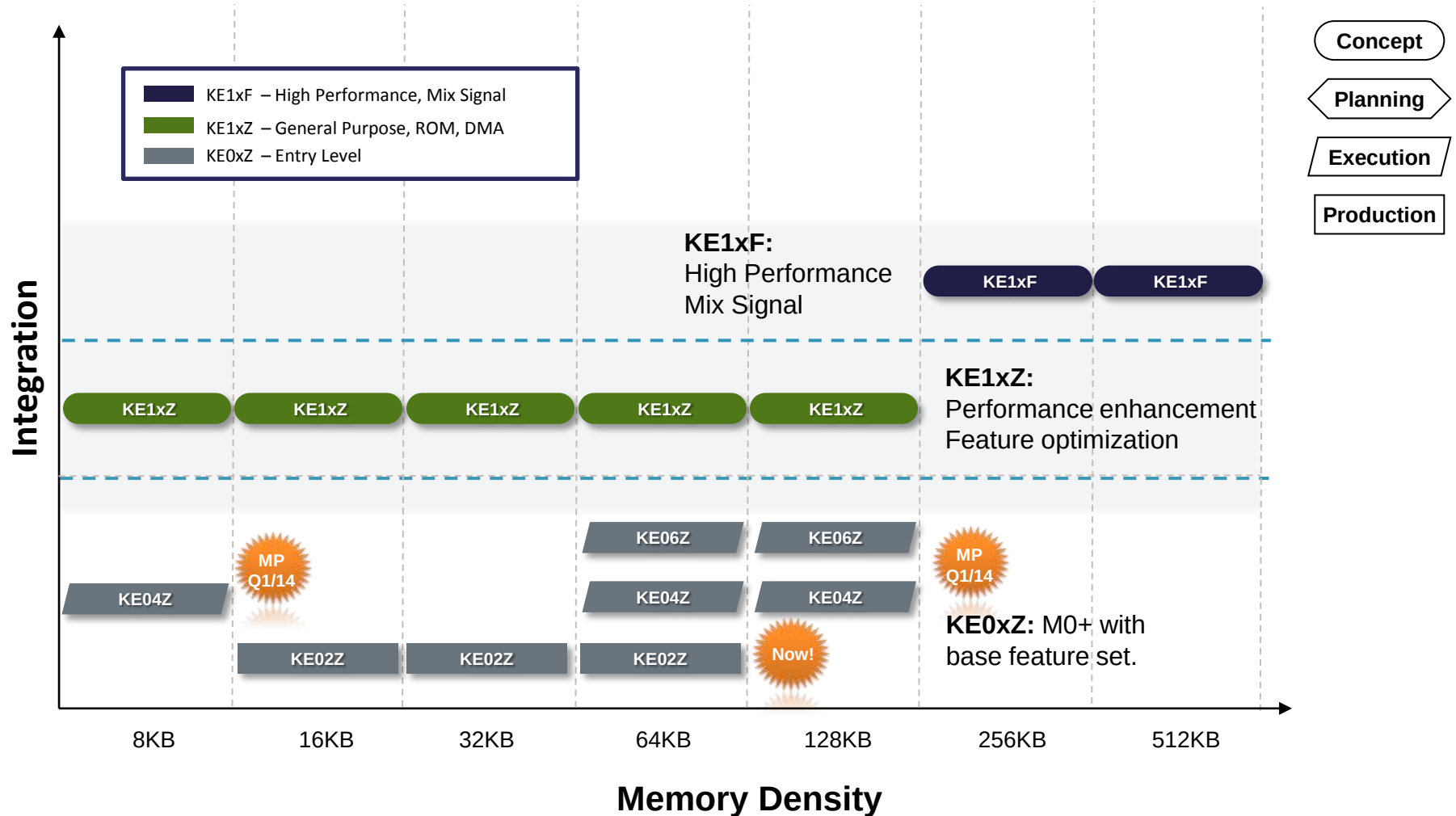
Where need **Robustness**

Timers 6ch Flex Timer 2 ch FlexTimer - PIT - PWT - RTC	System - PMU - Watchdog - LVD / POR - CRC - Bit manipulation engine	Core Complex - ARM Cortex™-M0+ Up to 48 MHz - Single cycle 32-bit x 32-bit multiplier - Single cycle I/O access port	Analog 12-bit ADC 2 x Analog Comparator Clocks 1% IRC - Ext OSC - FLL
Memory Interfaces - Up to 128KB Flash - Up to 512B EEPROM - Up to 16KB RAM	HMI - Up to 71 GPIO - KBI	Security 64-bit unique identification (ID) number	Serial Interfaces 3 x UART 2 x SPI 2 x I2C 1 x CAN

Where need **Low Cost** and **High Performance**

Kinetis E Series Product Roadmap

2.7-5.5V MCUs with high reliability and robustness, Based on ARM® Cortex-M® with best-in-class Enablement



Kinetis E-Series: MCU Families

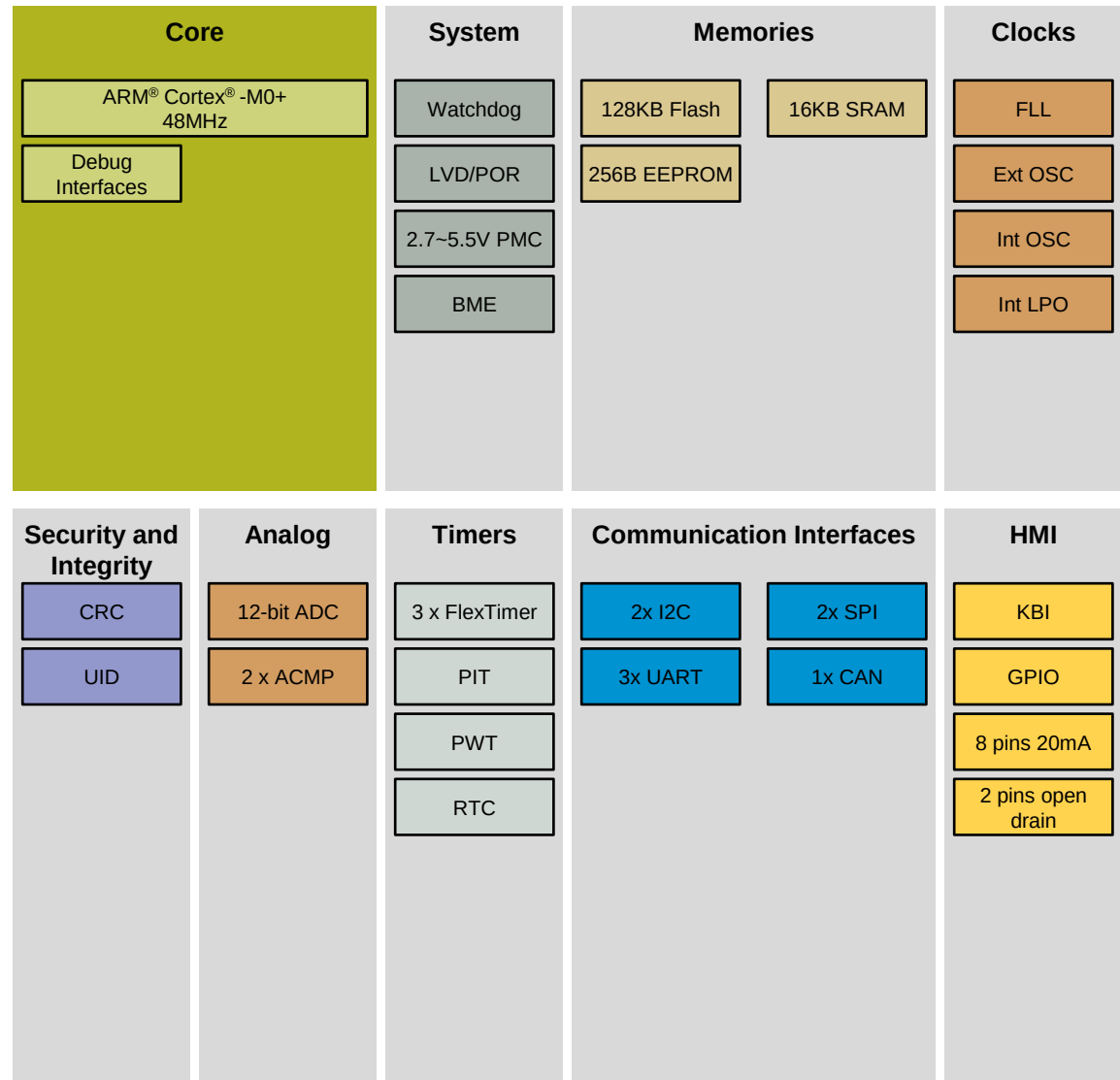
Common Features		Optional Features										
System		Family	Speed	Flash	SRAM	Key Features						
ARM Cortex-M0+ Core, 48MHz ^[1]						CAN	Seg. LCD	PWT	Fast Timer	ADC	TS	
Multiple power modes, Clock Gating, 2.7V – 5.5V												
Operating Temp: -40 to 105°C												
Clock Management		KE06Z	48MHz	64-128KB	8-16KB	✓		✓	✓	12-bit		
External OSC, 4~20MHz, 32KHz		KE04Z128	48MHz	128KB	16KB			✓	✓	12-bit		
Internal OSC, 32KHz, 1KHz												
Analog Peripherals		KE04Z64	48MHz	64KB	8KB			✓	✓	12-bit		
12-Bit ADC												
Analog Comparators		KE04Z8	48MHz	8KB	1KB			✓	✓	12-bit		
Serial Interfaces												
SCI		KE02Z	20MHz/ 40MHz	16-64KB	2-4KB					12-bit		
SPI, IIC												
Timers												
Real Time Clock												
16bit Flex timers												
32bit Periodic Interrupt Timer												

[1] 20MHz/40MHz for KE02

Kinetis E0x Series Master Block Diagram

Key Features:

- **Core/System**
 - ARM® Cortex® -M0+ up to 48MHz
- **Memory**
 - up to 128KB Flash
 - up to 16KB SRAM
- **Communications**
 - 1 x CAN
 - Multiple serial ports,
 - 3 x UART / 2 x SPI / 2 x I2C
- **Analog**
 - 16ch 12-bit ADC
 - 2x ACMP
- **Timers**
 - 1 x 6ch FTM
 - 2 x 2ch FTM
 - 1 x PIT
 - 1 x PWT
 - RTC
- **Others**
 - Up to 71 I/Os
 - 2.7-5.5V, -40 to 105°C
- **Packages:** 80/64/44/32 LQFP, 64QFP, 24QFN, 20SOIC, 16TSSOP
Pin compatible within KE



Kinetis E Series: Selling Point - Robust

Feature category	Feature	Benefit to customer
Robust	Improved 5V I/O pad with digital filter	Better EMC performance and system robust in the harness environment and easy for PCB layout
Safety	IEC60730 compliant watchdog, CRC and certified IEC60730 safety S/W library	Makes system more safer while reducing system cost by removing external BOM

Kinetis E Series: Selling Point - Efficiency

Feature category	Feature	Benefit to customer
Fast processing	Single cycle 32bx32b ARM Cortex-M0+ core	Much higher performance than M0, and 8/16-bit MCUs
Fast response	Nested Vectored Interrupt Controller	True hardware interrupt nesting and less interrupt latency than M0 and 8/16-bit MCUs
Fast response	12-bit x 16ch SAR ADC with 8-entry FIFO	Provide faster sampling rate, higher resolution, and faster response
Fast response	2x ACMP with 6-bit DAC	Provide over-current, over-voltage protection as well as zero-crossing detection for full voltage range.
Fast response	Bit manipulation engine	Support bit-band on peripherals that extends the core instructions and generates more efficient code
Fast response	Single cycle fast GPIO	Provide faster response bit-banging and software protocol emulation without additional BOM

Kinetis E Series: Selling Point - Application Special

Feature category	Feature	Benefit to customer
Motor control	6-ch 16-bit Flextimer optimized for motor control with sync to ADC via PDB	Make motor control easier
High drive	Up to 8 high drive pins with each supporting 20mA	Provide direct connection to LED drive circuit without additional cost
Data endurance	Up to 256B EEPROM with 500K endurance cycles	Provide longer life time of the NVM
SMBus	SMBus compatible IIC	Make SMBus connection easier without additional overhead

Kinetis E Series: Selling Point - Save Cost

Feature category	Feature	Benefit to customer
Scalable & Pin-Compatible	Wide range of packages with pin-compatible	Makes code easy to reuse and platform design easier
Low PCBA cost	0.8mm pitch package (64QFP)	Cost down PCBA process
Lost cost development tool	CW special edition free for 64KB	Cost down development

Kinetis E EMC Performance

Robustness in EFT,PESD and AC Power Relay Tests

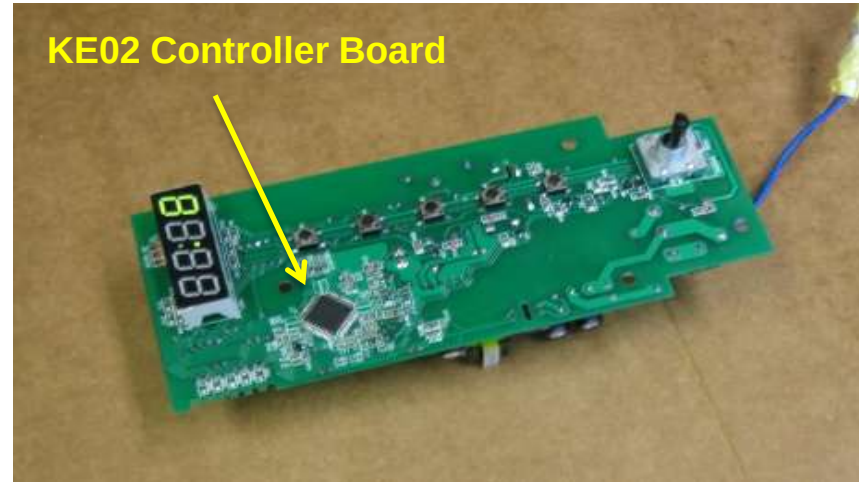
Test Conditions

- Microwave Oven Controller board with KE02 as main control MCU
- Board and System level tests based on
 - IEC 61000-4-4(EFT)
 - IEC 61000-4-2(PESD)
 - China Appliance local AC Power Relay test

Test Results

- Board level
 - IEC 61000-4-4(EFT): +/- 4.4kV*
 - IEC 61000-4-2(PESD): Indirect Contact
 - Discharge +/- 20kV
 - China Appliance local test on AC Power Relay:
 - 6-turns without Reset
- System level
 - IEC 61000-4-4(EFT): +/- 4.4kV*
 - IEC 61000-4-2(PESD): Contact
 - Discharge(at the case) +/- 20kV
 - IEC 61000-4-2(PESD): Air Discharge (at the control panel) +/- 15kV

*Limited by the test equipment max output voltage





Deep Dive of Key Features – Cortex-M0+

ARM Cortex-M0+ Processor:

The True 8-bit Replacement

- The smallest, lowest-power ARM processor on the market
- Compatible with all other Cortex-M cores
- The most energy-efficient 32-bit processor ever designed
- Single-cycle 32bx32b instruction
- Significant energy efficiency advantages over 8/16-bit
- Processor consumption as low as 9.8µW/MHz in 90nm process, or 52 µW/MHz in 180nm process
- Outstanding results of 1.77 CoreMark/MHz
- I/O low-power improvements with single cycle access to critical peripherals (GPIO ...)
- Relocatable vector table allows for dynamic exception handlers by moving the vector table into RAM
- Micro trace buffer brings fast debug advantages of trace to low-end MCUs (**not implemented in KE0x**)



ARM Cortex-M0+

*The next-generation
entry-level processor*

32-bit Performance and Functionality With 8-bit Ease-of-Use

**Super
Simple**

CoreMark Code in kB



Streamlined Architecture

The new cortex-M0+ core strikes the right balance of performance and simplicity needed in entry-level applications.

Accelerated Debugging

Micro trace buffer accelerates software debug without wasting additional I/O. Plus, get faster bug identification and correction with minimal system resources. (Micro trace buffer not implemented in KE0x)

Closer to the Hardware

Single-cycle IO and peripheral bus facilitate bit-banding and software protocol emulation, keeping it an 8-bit 'look and feel'.

Ultimate Code Density

Cortex-M0+ instruction set provides the most compact code even when compared to legacy 8- and 16-bit architectures. Do more with the same Flash size.

CoreMark code compiled optimized for size. A, B, C & D

Benefits of Moving from 8/16-bit to 32-bit ARM Cortex-M0+

8/16-bit

Performance

- Older, slower architectures & technology
- Increased code size/complexity when performing complex math operations

Energy-Efficiency

- Low energy-efficiency

Low Cost

- 6-35k gates
- Variable code density

Ease-of-Development

- Limited addressable memory
- Simplistic interrupt controllers
- Limited scalability (MHz, flash, features)
- Limited ecosystem support

32-bit ARM Cortex-M0+

Performance

- 2x to 40x more than 8/16-bit, 9% more than Cortex-M0
- Fast 32-bit math processing
- Fast single-cycle access to I/O

Energy-Efficiency

- >2x CoreMark/mA than closest 8/16-bit MCU, +30% / CM0

Low Cost

- 12-35k gates
- Excellent code density

Ease-of-Development

- Linear 4GB address space – no need for paging
- Full-featured interrupt controller – simpler s/w architecture
- Huge scalability – h/w and s/w reuse across end products
- Huge ARM ecosystem – off-the-shelf software/tools/training
- Micro Trace Buffer – lightweight, non-intrusive trace (not implemented in Kexx)

Cortex-M Processor Family

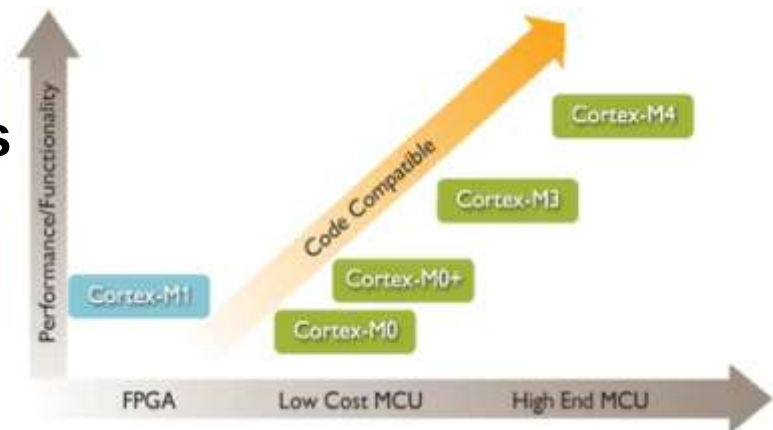
Five products, two architectures

Cortex-M4	High performance data processing & I/O control. Support hardware divide, MAC, bit field processing, DSP. Floating point unit optional (Cortex-M4F).	ARMv7-M architecture
Cortex-M3	High performance data processing & I/O control. Support hardware divide, MAC (Multiply Accumulate) , bit field processing.	
Cortex-M0+	General data processing, high performance I/O control, mixed signal ASICs, replacement for 8/16-bit MCUs	ARMv6-M architecture
Cortex-M0	General data processing, I/O control, mixed signal ASICs, replacement for 8/16-bit MCUs	
Cortex-M1	For FPGA designs only. Optimized for FPGA and can work in most FPGA devices	



Common Features

- **Many features are available on all Cortex-M Microcontrollers**
 - **NVIC** - Nested Vector Interrupt Controller
 - **Sleep modes and low power features**
 - **OS support** features such as **SysTick** timer
 - **CMSIS-Core** support (API software for processor feature)
 - **Debug** support
 - Different subset of **Thumb-2** Instruction Set Architecture
- **Architecture consistency means**
 - Using the same tool chain
 - Easy program code reuse
 - Multi-sources possible



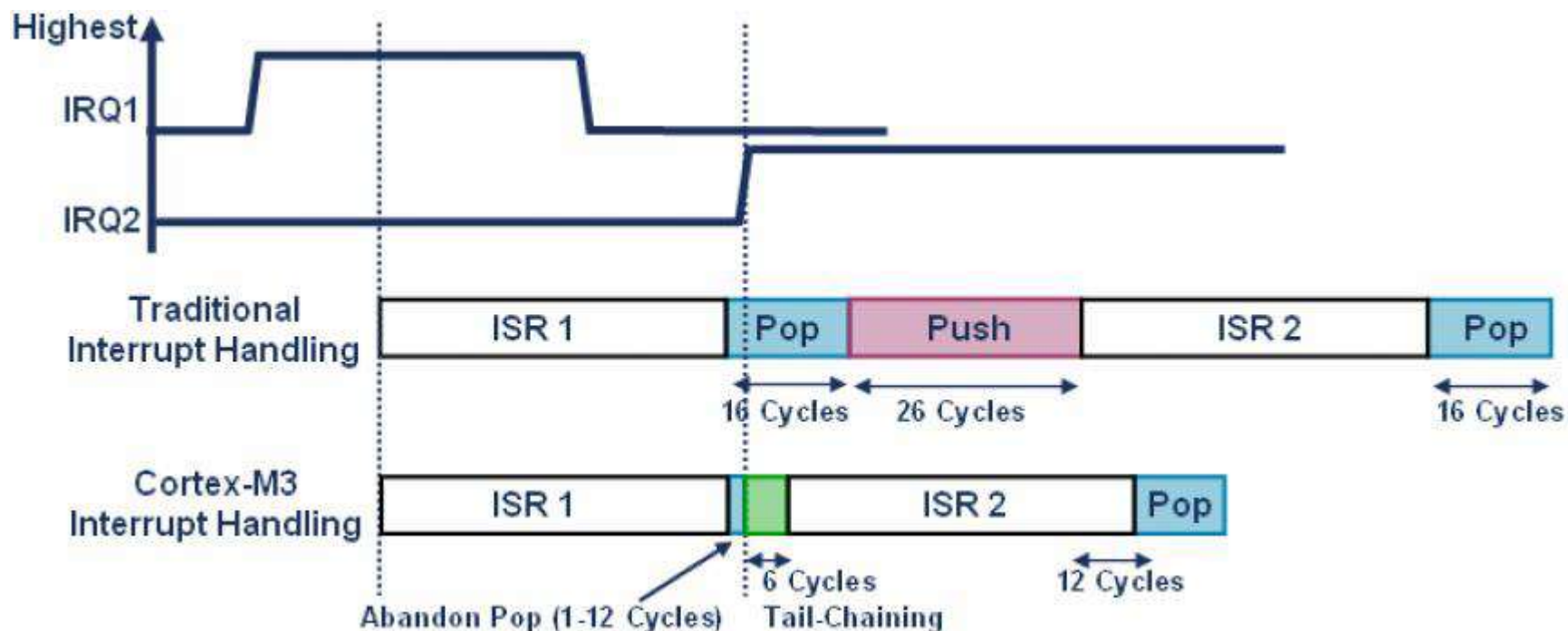
NVIC Feature Comparisons

NVIC features	Cortex-M0	Cortex-M0+	Cortex-M3	Cortex-M4
Max Number of IRQ	32 + NMI	32 + NMI	240 + NMI	240 + NMI
System exceptions	4	4	8	8
Exception Priority levels	4(prog) + 2 (fixed)	4(prog) + 2 (fixed)	8 to 256(prog) +2(fixed)	8 to 256(prog) +2(fixed)
Masking registers	1	1	3	3
Interrupt Latency (cycles)	16	15	12	12
Dynamic priority change	No	No	Yes	Yes
Vector table relocation	No	Yes (optional)	Yes	Yes
Register accesses	32-bit	32-bit	8/16/32-bit	8/16/32-bit

Interrupt Controller (NVIC)

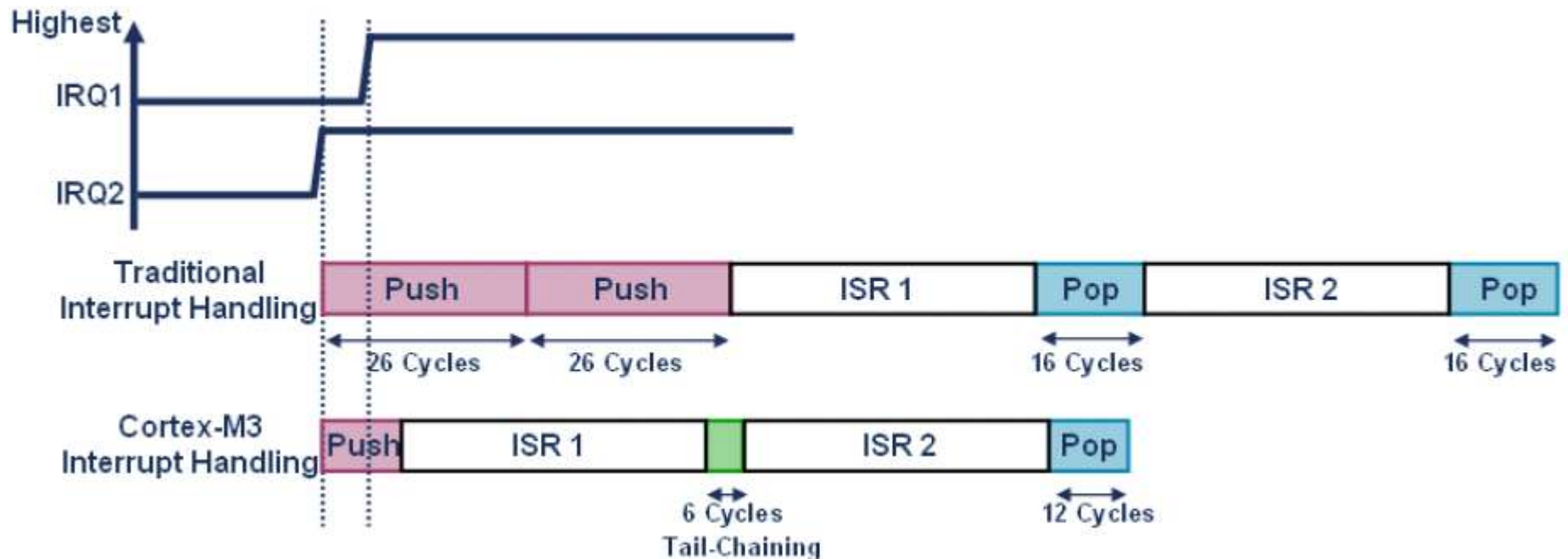
- The Cortex-M family uses a number of methods to improve interrupt latency. The first one is called tail chaining. And the second method is called late arrival. The third one is **Stack pop pre-emption**.

❖ Tail chaining operation



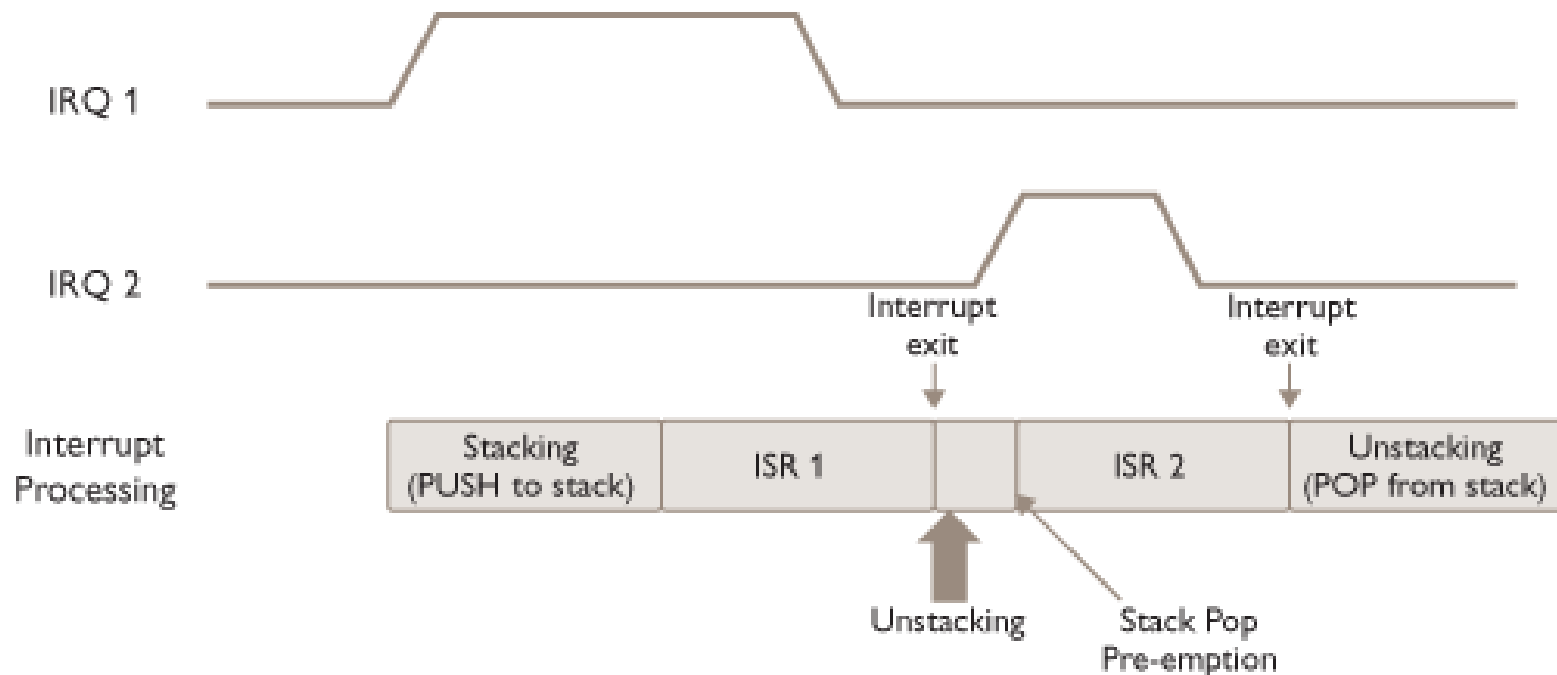
Interrupt Controller (NVIC)

- Late arrival operation



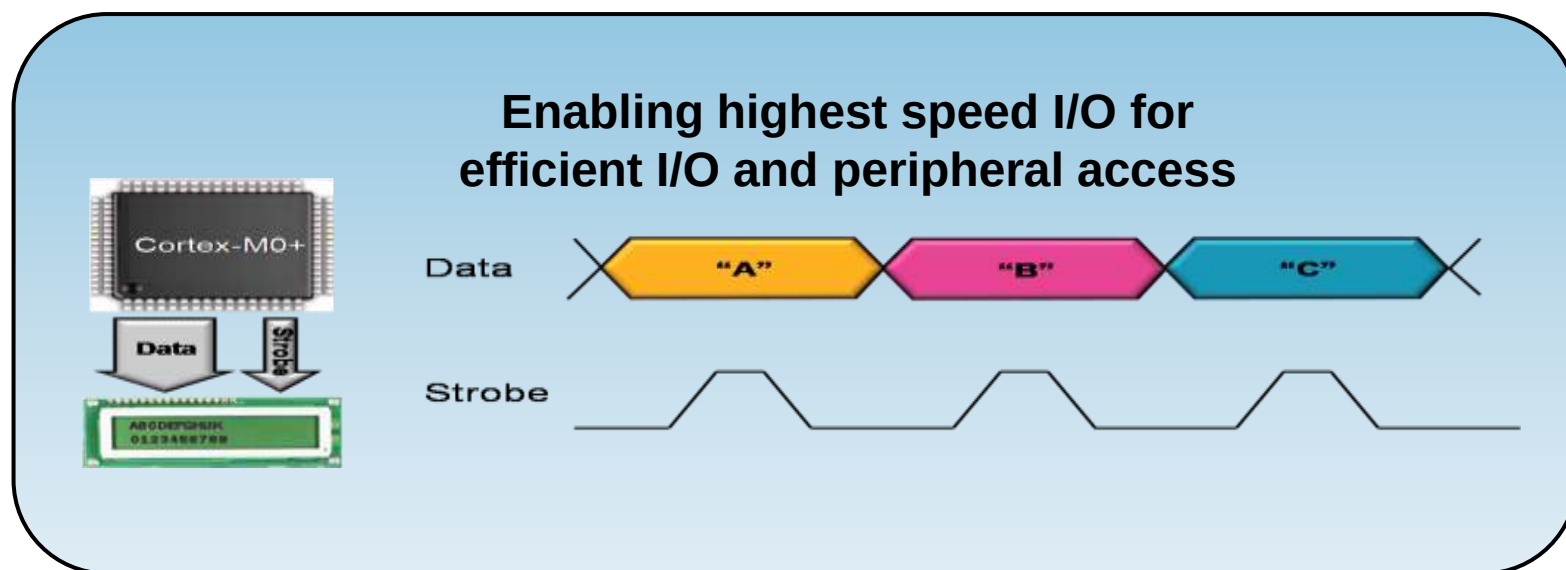
Interrupt Controller (NVIC)

- Stack pop pre-emption operation



Single cycle GPIO

- Provide faster response bit-banging and software protocol emulation without additional BOM
- Up to **50%** faster than normal I/O
- Fast GPIO controller (FGPIO) have SET/CLEAR/TOGGLE control for all pins in zero wait states





Other Key Features

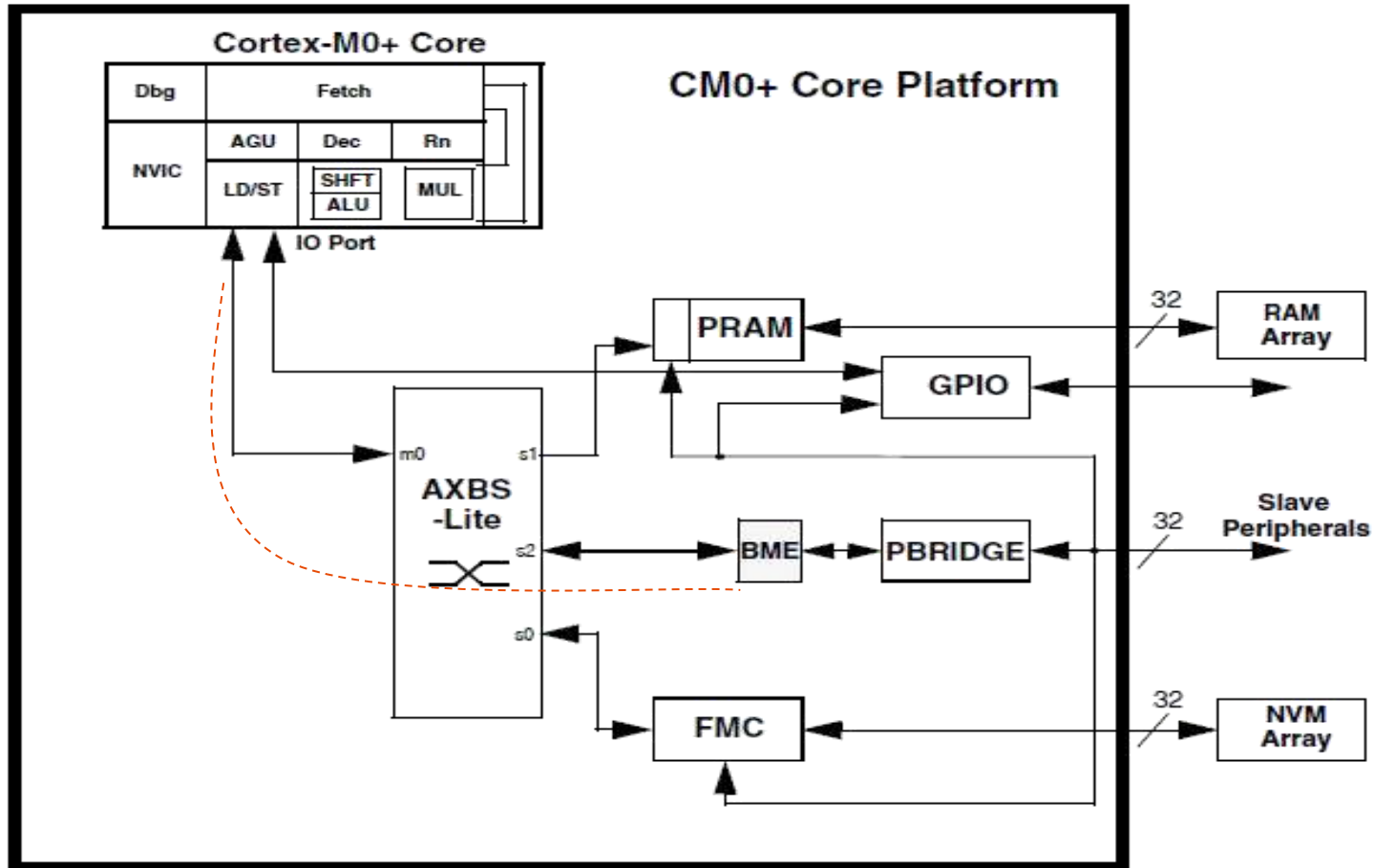
Bit Manipulation Engine

- The BME is a hardware block that resides between the platform and E-Series Core that allows read-modify-write operations to be performed on peripheral registers using data stored in the target address
 - Decorated Stores
 - AND, OR, XOR and Bit field insert (BFI)
 - Decorated Loads
 - Load and clear one bit (LAC1), Load and Set one bit (LAS1), Unsigned bit field extract (UBFX)



Bit Manipulation Engine (BME)

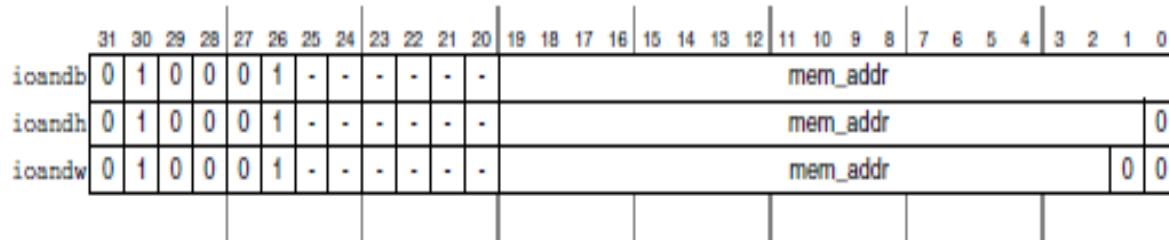
BME decorated references are only available on system bus transactions generated by the processor core



Note: BME can be accessed only by the core.

Example: Decorated Store Logical AND

- The data size is specified by the write operation and can be byte (8 bit), halfword (16 bit) or word (32 bit). The core performs the required write data lane replication on byte and halfword transfers



- where $\text{addr}[28:26] = 001$ specifies the AND operation, and $\text{mem\_addr}[19:0]$ specifies the address offset into the peripheral space based at $0x4000\_0000$. The "-" indicates an address bit "don't care".
- Typical operation
 $\text{GPIOA\_PDOR} \&= 0x02$
- BME operation
 $*(\text{unsigned long } *)0x440ff000) = 0x02$

BME vs C code for Bit field insertion with highest speed optimization

- C code for bit field insertion without BME

```
0x1128: 0x6ae0    LDR    R0, [R4, #0x2c]
0x112a: 0x4028    ANDS   R0, R0, R5
0x112c: 0x21a0    MOVS   R1, #160          ; 0xa0
0x112e: 0x02c9    LSLS   R1, R1, #11
0x1130: 0x4301    ORRS   R1, R1, R0
0x1132: 0x62e1    STR    R1, [R4, #0x2c]
```

11
cycles,
12 bytes

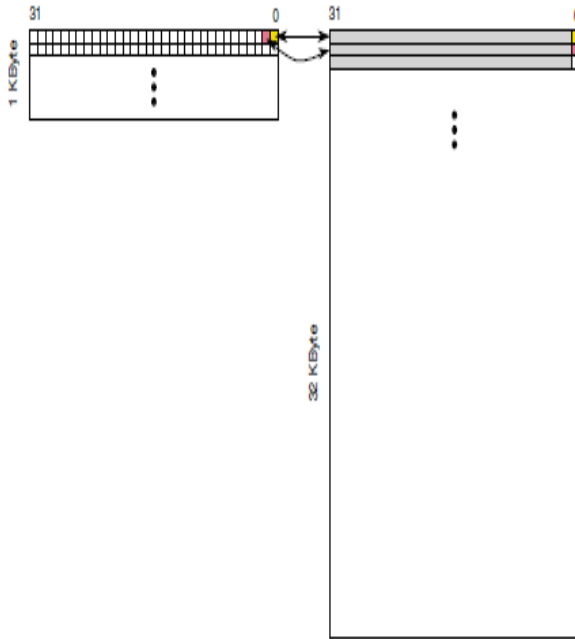
- C code for bit field insertion with BME

```
BME_BITFIELD_INSERT(u32Addr,16,4) = u32Data; /* write 5 to bit 19..16 */
0x115e: 0x482d    LDR.N   R0, ??DataTable14_9    ; 0x5818f040
(1478029376)
0x1160: 0x21a0    MOVS   R1, #160          ; 0xa0
0x1162: 0x02c9    LSLS   R1, R1, #11
0x1164: 0x6001    STR    R1, [R0]
```

10
cycles,
8 bytes

Speed improved by 9%
Code size improved by ~33%

Bit-band (KE04 and KE06)

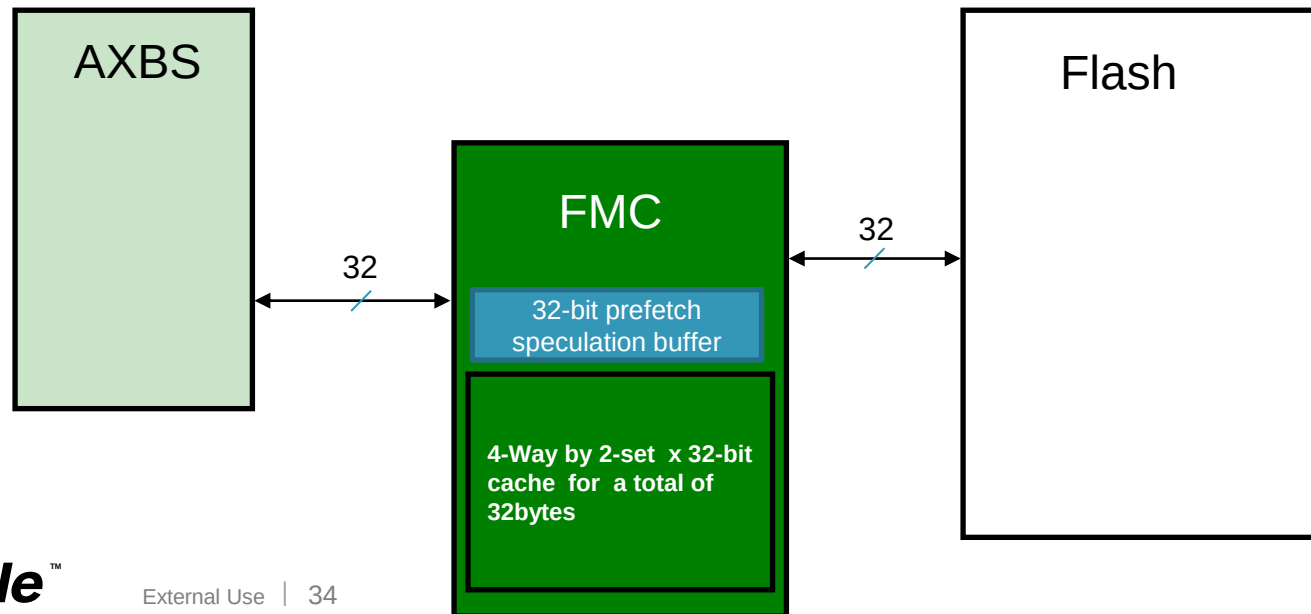


- Support uninterruptible atomic read-modify-write operation on RAM-U
- Two 32 MB aliased bit-band regions associated with the two 1 MB bit-band spaces, functional on RAM-U
- Each 32-bit location in the 32 MB space maps to an individual bit in the bit-band region
- A 32-bit write in the alias region has the same effect as a read- modify- write operation on the targeted bit in the bit-band region
 - A 32-bit write in the alias region returns either
 - Writing a value with bit 0 set writes a 1 to the target bit.
 - Writing a value with bit 0 clear writes a 0 to the target bit.
 - A 32-bit read in the alias region returns either
 - a value of 0x0000_0000 to indicate the target bit is clear
 - a value of 0x0000_0001 to indicate the target bit is set



FLASH Memory Controller: FMC

- The FMC sits between the platform masters (Core) and the Flash, accelerates access time with buffers which will provide 0 wait state access times when hit.
- Each access of the Flash pulls next 32-bits into the FMC cache buffer, This way we move 2 instructions and can deliver full performance to the 48MHz bus from the 24Mhz Flash bus.
- When flash cache enabled, the power consumption is also improved



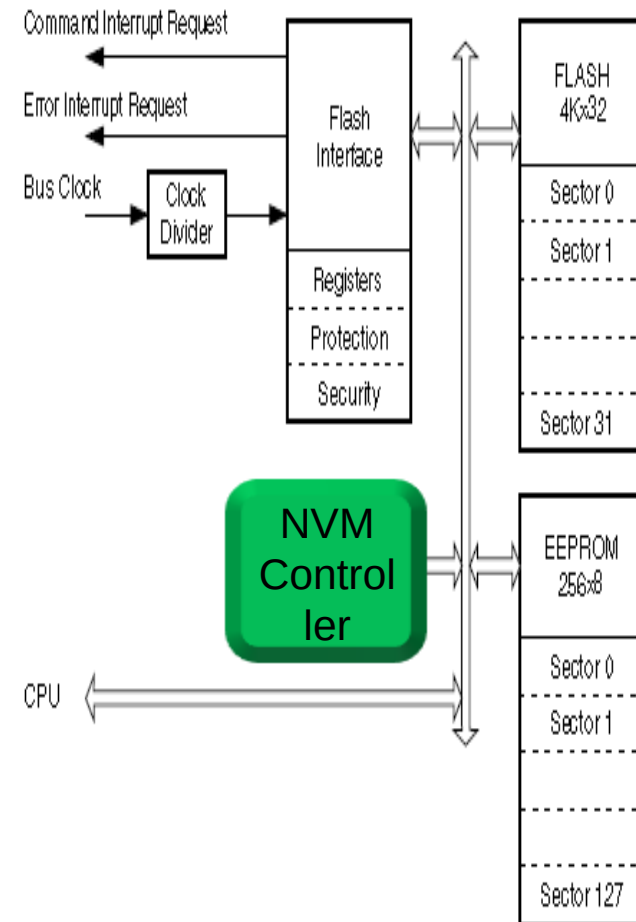
Flash and EEPROM

- **Flash memory**

- 64-bit security and backdoor key
- Automated program and erase algorithm with verify
 - Fast sector erase (sector size = 512B) and longword (32-bit) program operation
 - Flexible protection scheme to prevent accidental program or erase of flash memory
- Accessible 64-byte in hidden non-volatile information block
- Ability to set flash read margin levels

- **EEPROM**

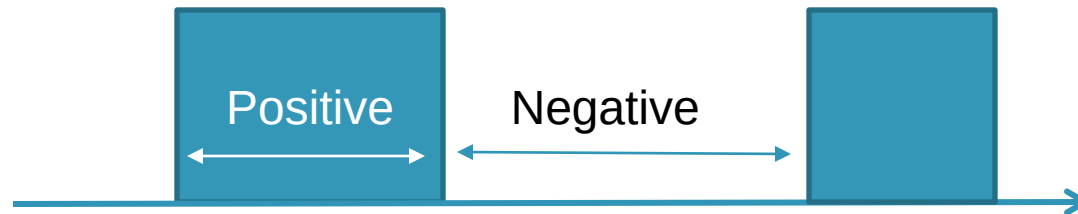
- Single-bit fault correction and double-bit fault detection within a word during read operations
- Automated program and erase algorithm with verification and generation of ECC parity bits
- Fast sector erase (sector size = 2B) and byte program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four bytes in a burst sequence
- Ability to set EEPROM read margin levels
- 500K program/erase cycles



KE0x family has another new flash operation feature: read-while-write. It allows read from flash while programming/erasing the flash by setting Enable Stalling Flash Controller bit in MCM_PLACR

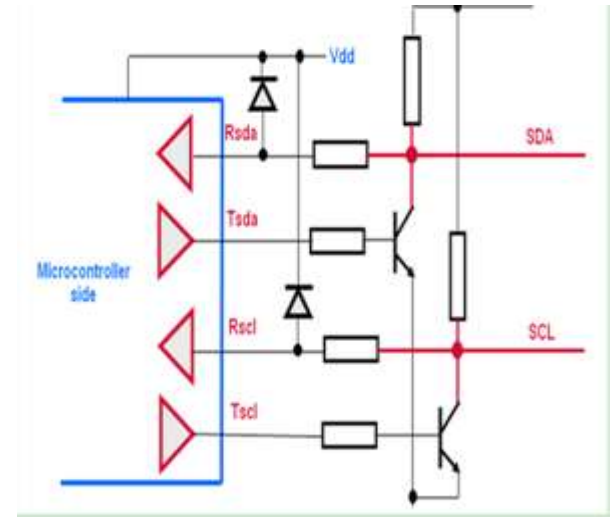
Pulse Width Timer (PWT)

- Capture signal period/frequency directly by h/w in 16-bit resolution
- Provide highest response to system
- Reduce CPU overhead
- Can measure positive and/or negative pulse width
- Programmable triggering edge for starting measurement
- Programmable measuring time between successive alternating edges, rising edges or falling edges
- Programmable prescaler from clock input as 16-bit counter time base
- Two selectable clock sources—bus clock and alternative clock
- Four selectable pulse inputs
- Programmable interrupt generation upon pulse width value updated and counter overflow



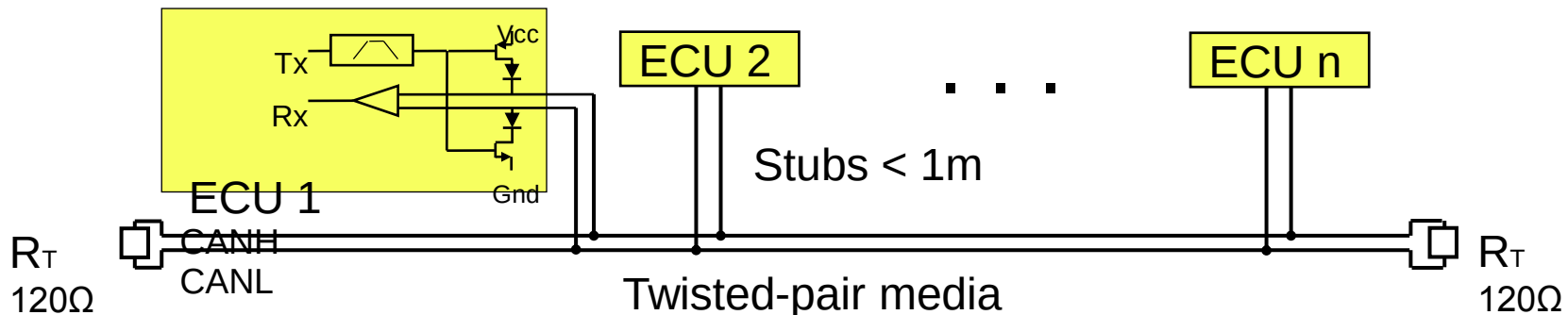
4-wire I²C support

- Flexible to interface with external custom line drivers
- Provide higher bus drive capability
- Provide higher noise immunity in EMC environment
- Reduced total system BOM
- SMBus spec v2 compatible
- 5-bit glitch input filter
- Range slave address recognition
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Programmable glitch input filter
- Low power mode wakeup on slave address match
- Can be disabled to support traditional 2-wire bi-dir I²C

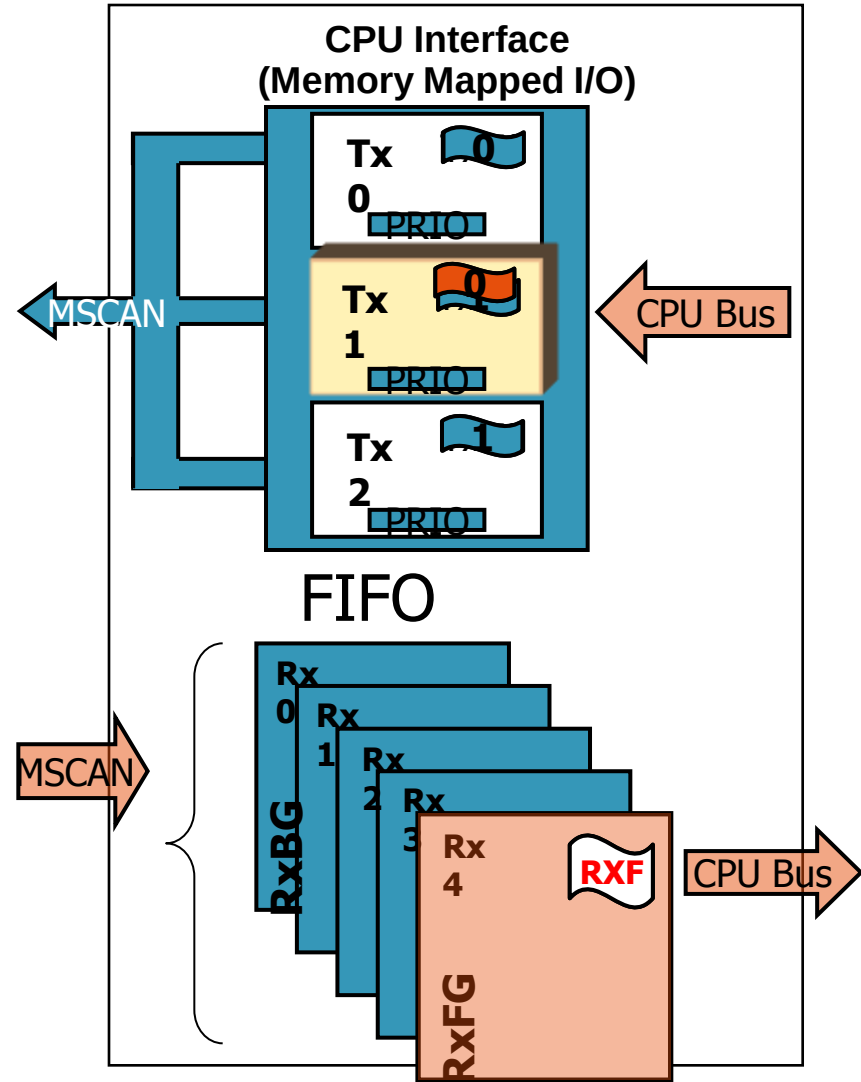
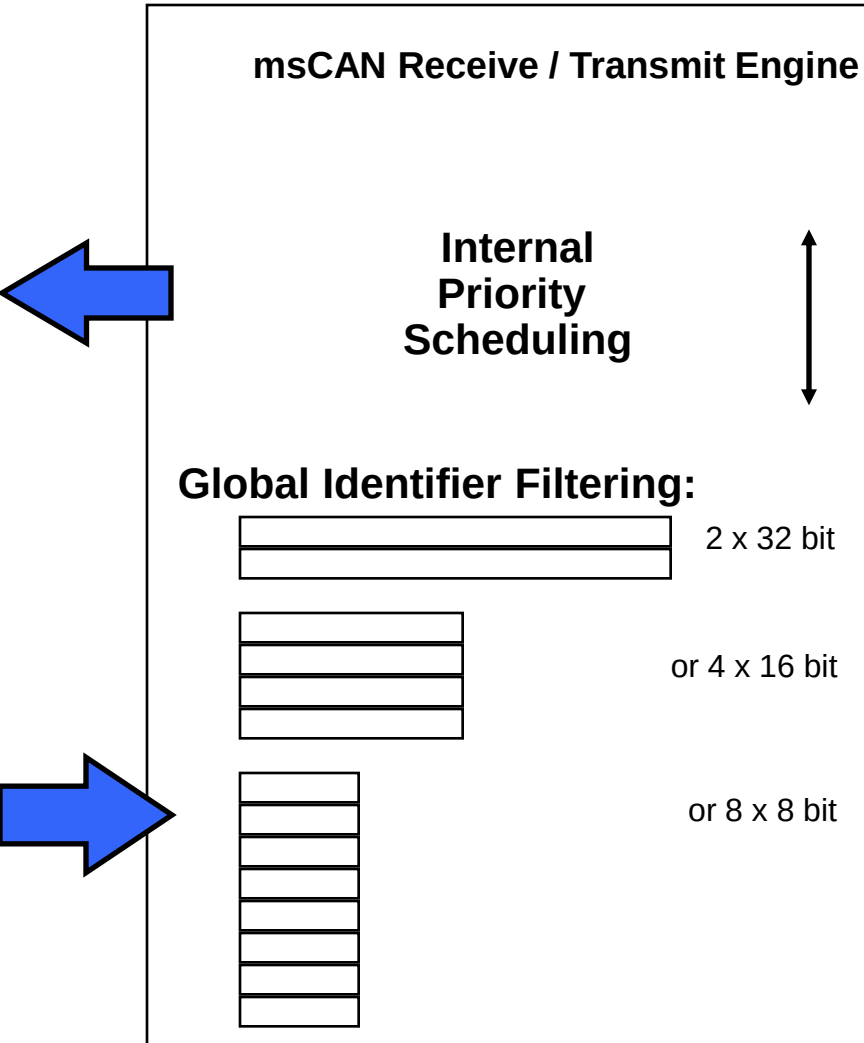


Controller Area Network (CAN)

- Fully compliant with CAN 2.0A/B protocol
- Automotive proven leading edge CAN controller popular in tough noise EMI environment
- 5 Receive buffers with FIFO storage scheme
- 3 Transmit buffers with internal prioritization using a 'local priority' concept
- Flexible maskable identifier filters to receive wanted messages
- Programmable functionality:
 - Wake-up with integrated low-pass filter
 - Loop-back mode supports self-test operation
 - Listen-only mode for monitoring of CAN bus
 - bus-off recovery functionality
- Separate signaling and interrupt capabilities for all CAN receiver and transmitter error states (Warning, Error Passive, Bus-Off)
- Programmable clock source either system clock or crystal oscillator output
- Internal timer for time-stamping of received and transmitted messages
- Low power modes: Sleep, Power Down and MSCAN Enable



Controller Area Network (CAN)



IEC60730 Safety Standard Class B Cert. for Household Appliance

- IEC60730 safety standard classification:
 - Class A: Not intended to be relied upon for the safety of the equipment
 - Class B: To prevent unsafe operation of the controlled equipment
 - Class C: To prevent special hazards

Test	IEC 60730 Class B				IEC 60730 Class C		
IEC 60730 periodic test	8-bit S08	16-bit DSC568XXX	32-bit MCF51xx	32-bit Kinetis	8-bit S08	16-bit DSC568xxx	32-bit MCF51xx
CPU register test	Stuck at	Stuck at	Stuck at	Stuck at	Walkpat	Walkpat	Walkpat
CPU instruction test	N/A	N/A	N/A	N/A	CPU instr. test	CPU instr. test	CPU instr. test
RAM test	March C, X	March C	March C	March C, X	Walkpat	Walkpat	Walkpat
Flash test	CRC 16-bit	CRC 16-bit	CRC 16-bit	CRC 16-bit	CRC 16-bit	CRC 16-bit	CRC 16-bit
Watchdog test	Timeout and reset	Timeout and reset	Timeout and reset	Timeout and reset	Timeout and reset	Timeout and reset	Timeout and reset

IEC60730 Safety Standard Class B Cert. for Household Appliance

- IEC60730 safety standard peripherals
 - **Watchdog**: independent clock source and robust refresh & protection mechanism, provide safety mechanism to monitor
 - The flow of the software
 - Interrupt handling & execution
 - CPU clock (too fast, too slow and no clock)
 - **Cyclic Redundancy Check (CRC)**: provides a fast mechanism for
 - Testing the Flash memory
 - Check on serial communication protocols (UARTS, I2C, SPI)

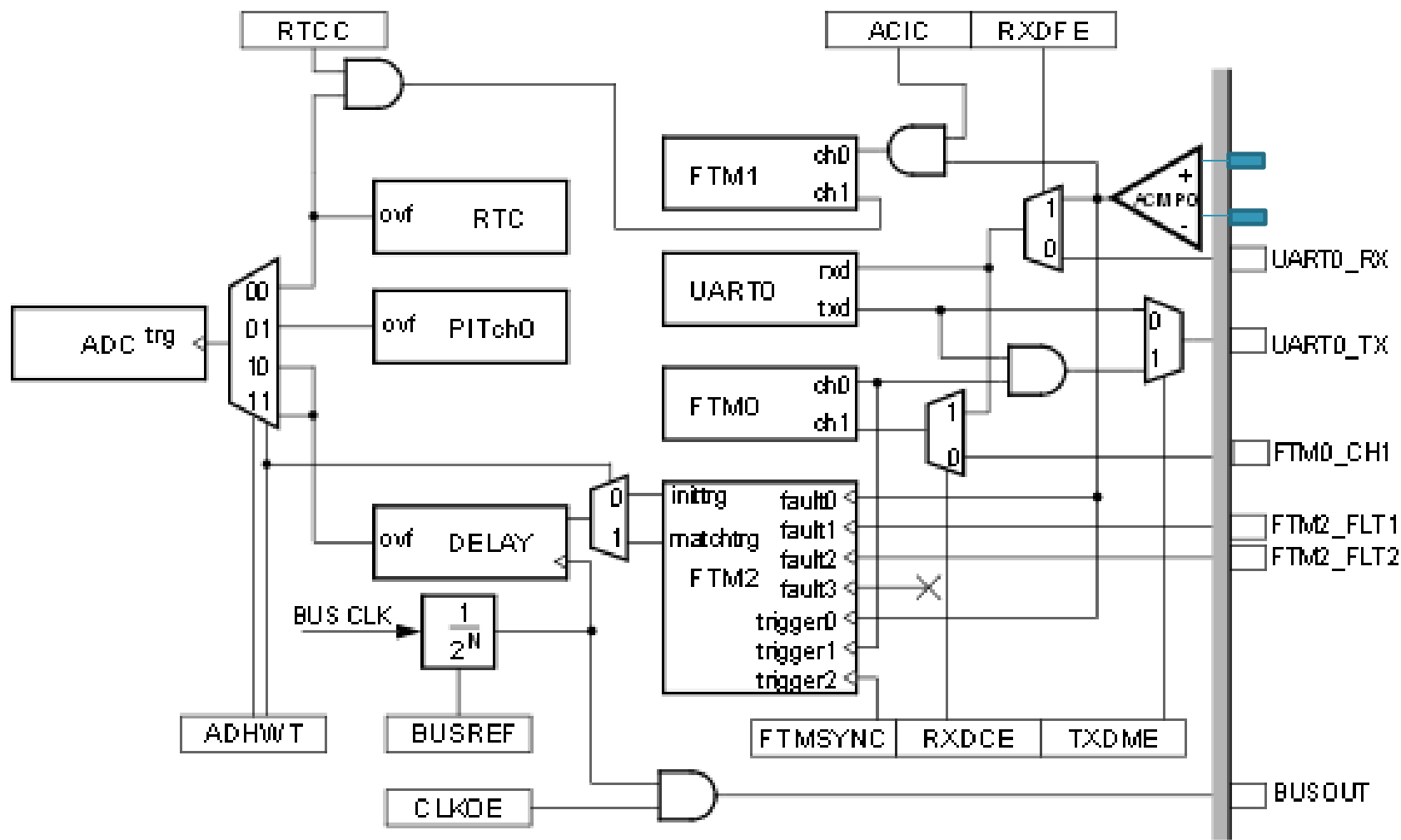
Simple Power Mode

Core power mode	System/chip power Mode
RUN	RUN
Sleep	WAIT
Deep sleep	STOP

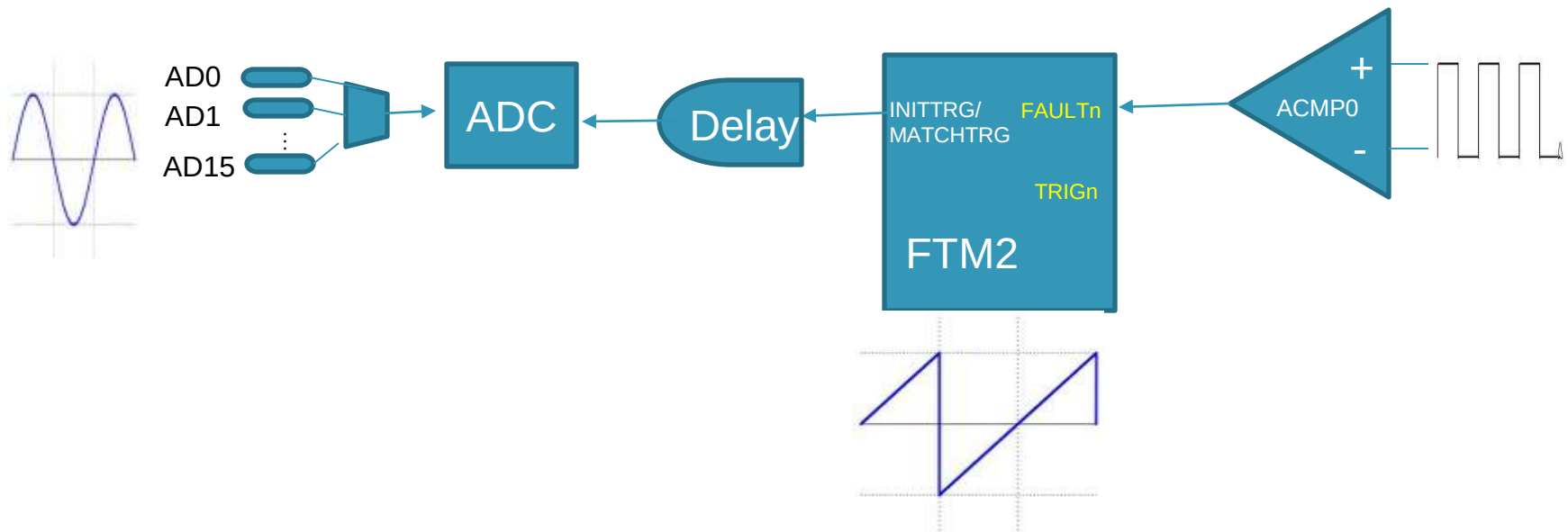
type	condition	core/bus clock	VDD	clock gating	IDD
WIDD	Wait mode, run code in Flash	40M:20M	5V	ON	7.46mA
				OFF	5.98mA
			3V	ON	6.51mA
				OFF	5.03mA
		20M:20M	5V	ON	6.95mA
				OFF	5.47mA
			3V	ON	6.01mA
				OFF	4.53mA
SIDD	LVD off	-	5V	-	1.2uA
		-	3V	-	1.1uA
	LVD on	-	5V	-	126.8uA
		-	3V	-	122.8uA
	LVD off, ADC on	-	5V	-	39.7uA
		-	3V	-	39.2uA

type	condition	core/bus clock	VDD	clock gating	IDD
RIDD	run code in Flash FEI mode	40M:20M	5V	ON	10.70mA
				OFF	9.23mA
			3V	ON	9.75mA
				OFF	8.27mA
		20M:20M	5V	ON	8.53mA
				OFF	7.04mA
			3V	ON	7.60mA
				OFF	6.10mA
RIDD	run code in Flash FEI mode enable most modules	40M:20M	5V	ON	11.19mA
			3V	ON	10.24mA
		20M:20M	5V	ON	8.94mA
			3V	ON	8.01mA
RIDD	run code in Flash FEI mode enable most modules while to access SRAM	40M:20M	5V	ON	13.96mA
			3V	ON	12.83mA
		20M:20M	5V	ON	11.265mA
			3V	ON	10.246mA

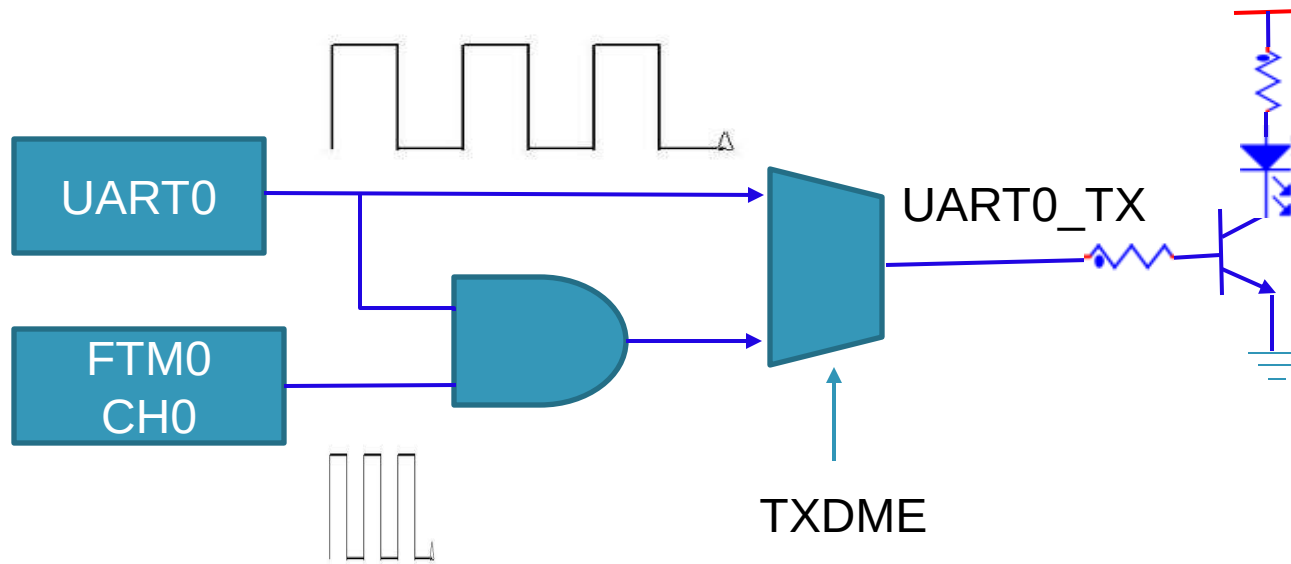
Module to Module Interconnection



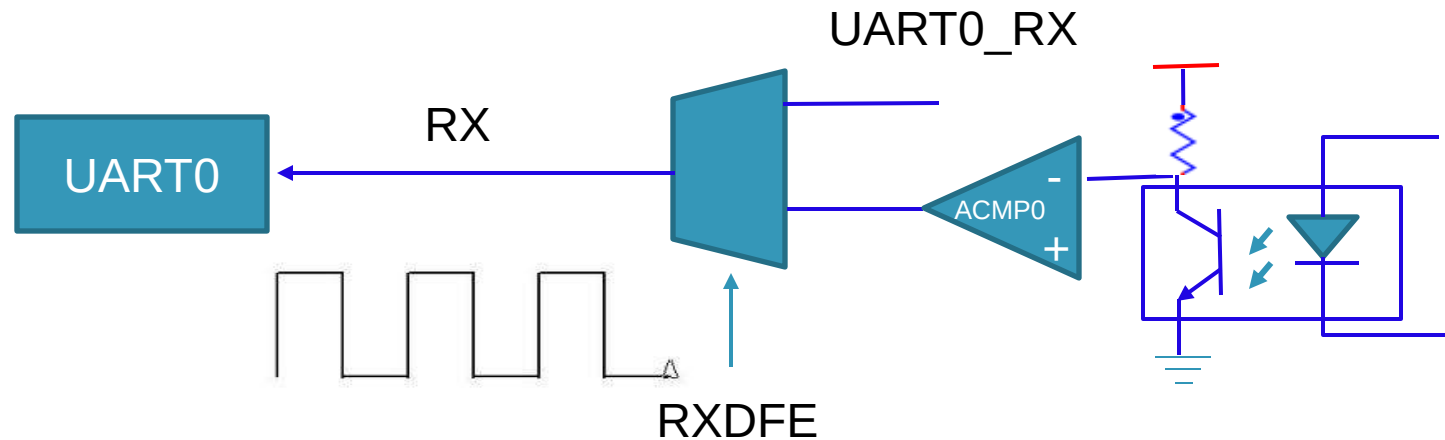
Use case1: FTM2 sync ADC while ACMP generates fault to FTM2



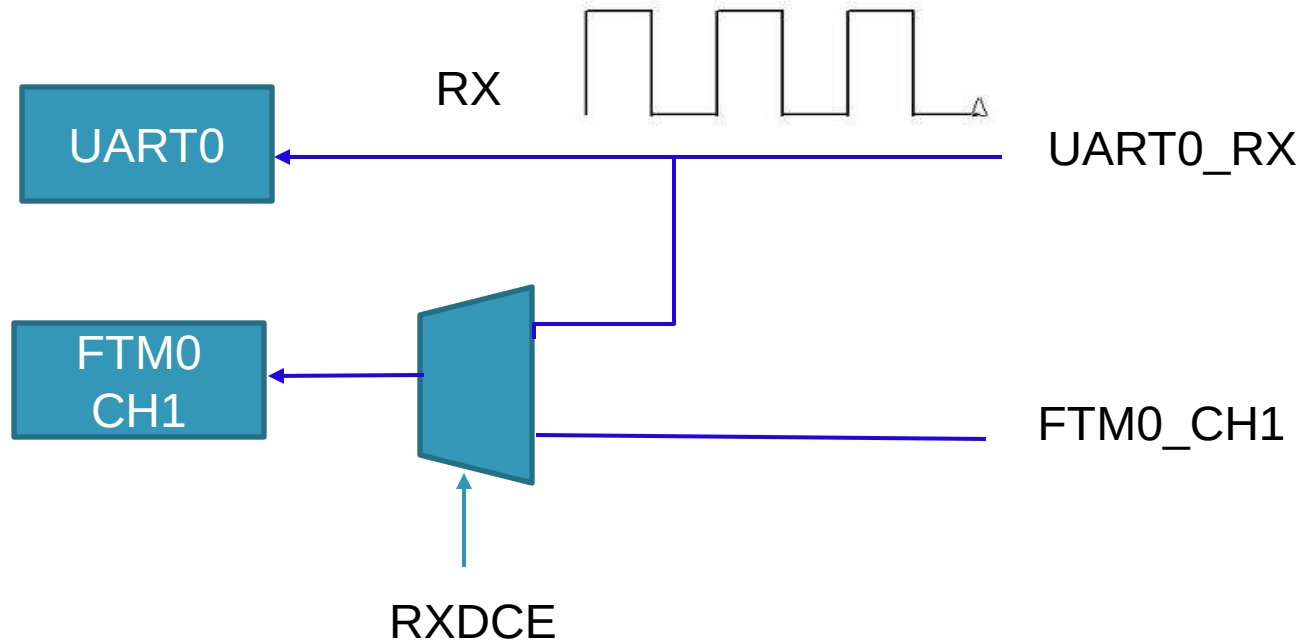
Use case2: UART0 TXD modulation for Infrared



Use case3: UART0 RX filter for Infrared demodulation

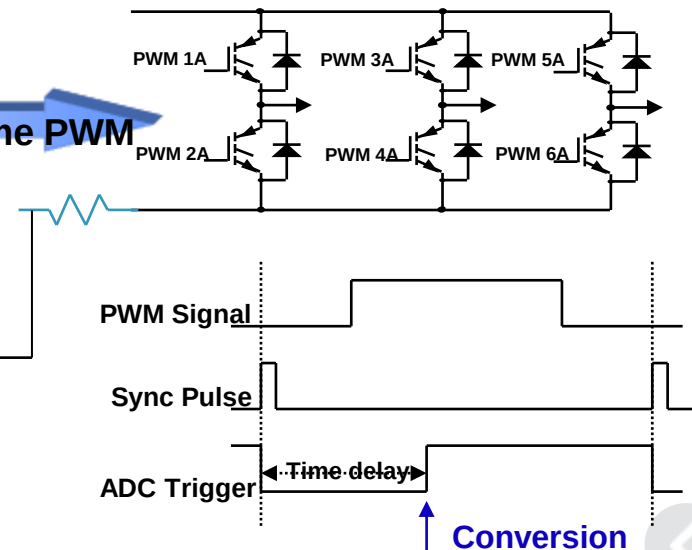
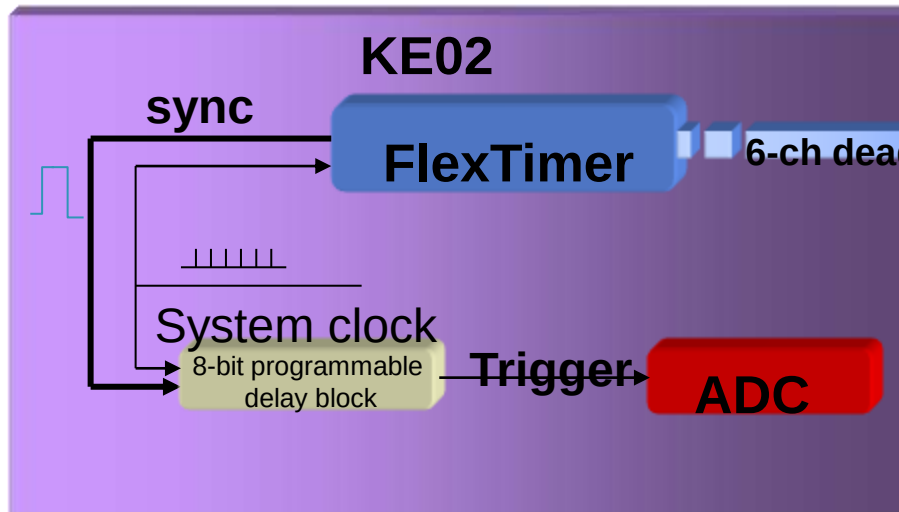


Use case4: UART0 RX capture by FTM0 ch1



Fast FlexTimer (FTM)

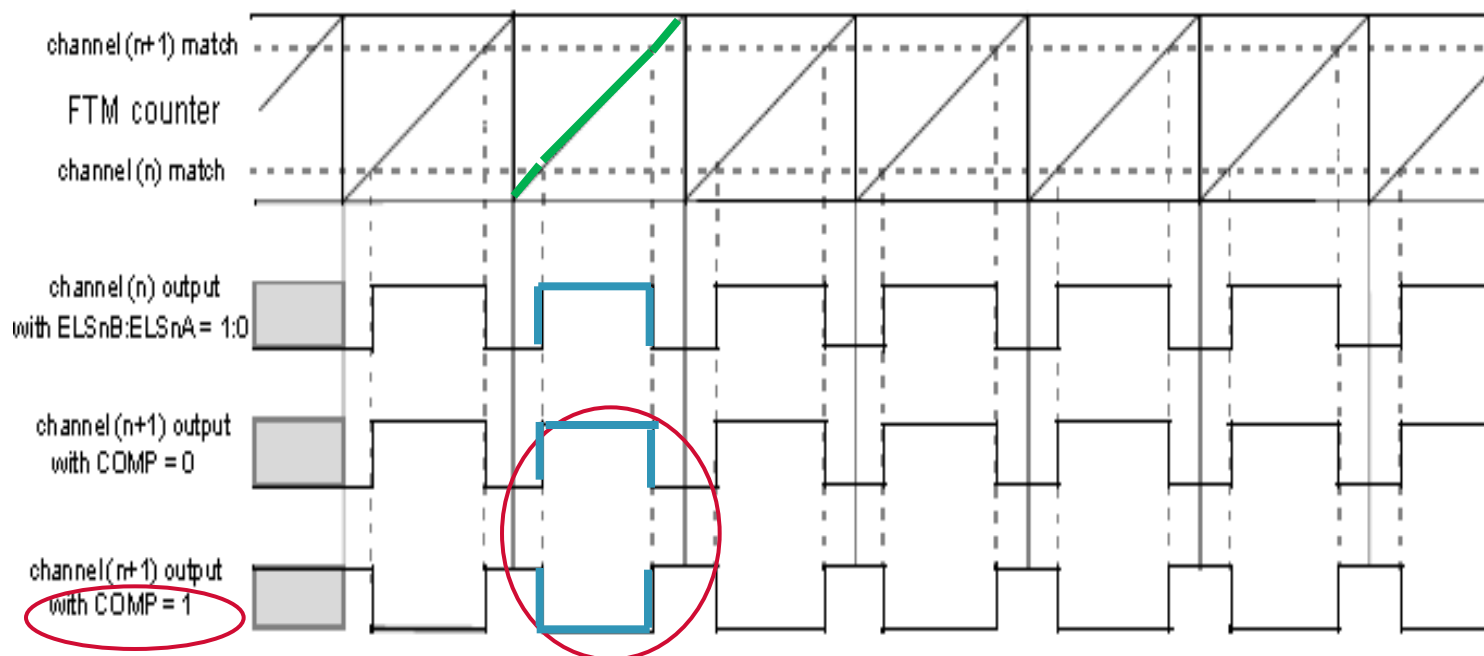
- Optimized for motor control and power conversion applications
- FTM clock as high as CPU clock (up to 48MHz)
- Generation of independent, complementary and asymmetric PWM
- Hardware dead time insertion
- Rich PWM synchronization scheme and fault protection
- PWM output masking and polarity control
- Enhanced triggering functionality (channel match trigger and init trigger)
- Dual edge capture
- Immediate PWM registers load
- Invert control/channel swap
- Fault input polarity control
- Programmable TOF frequency
- Software output control
- Debug mode function (The FTM can be set to still function when the debug mode is entered)
- Can sync with ADC via programmable delay block



FlexTimer

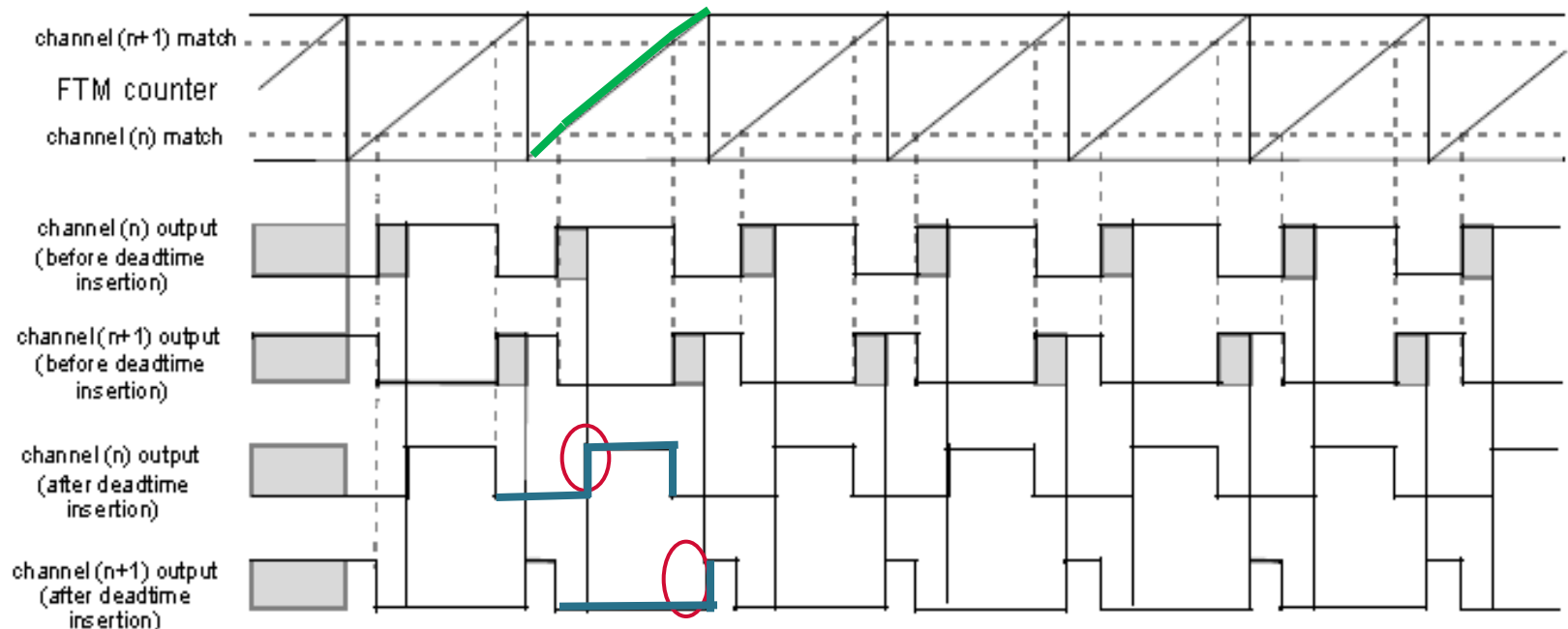
- Complementary PWM

- Channel $<n>$ controls first edge of PWM, while $<n+1>$ controls 2nd PWM edge



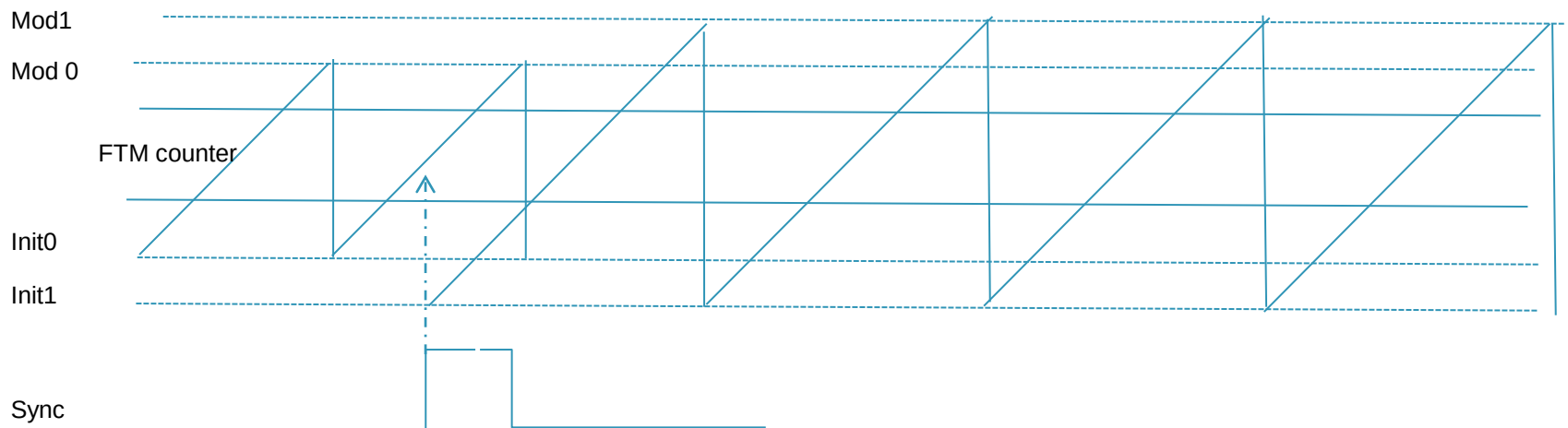
FlexTimer

- Deadtime insertion
 - Deadtime insertion on either rising edge or falling edge
 - Counter clock derived from 1/4/16 system clocks
 - Count from 1 to 63
 - Dead time from 1 to 1008 system clocks (0.05 to 50.4us @20MHz)



FlexTimer

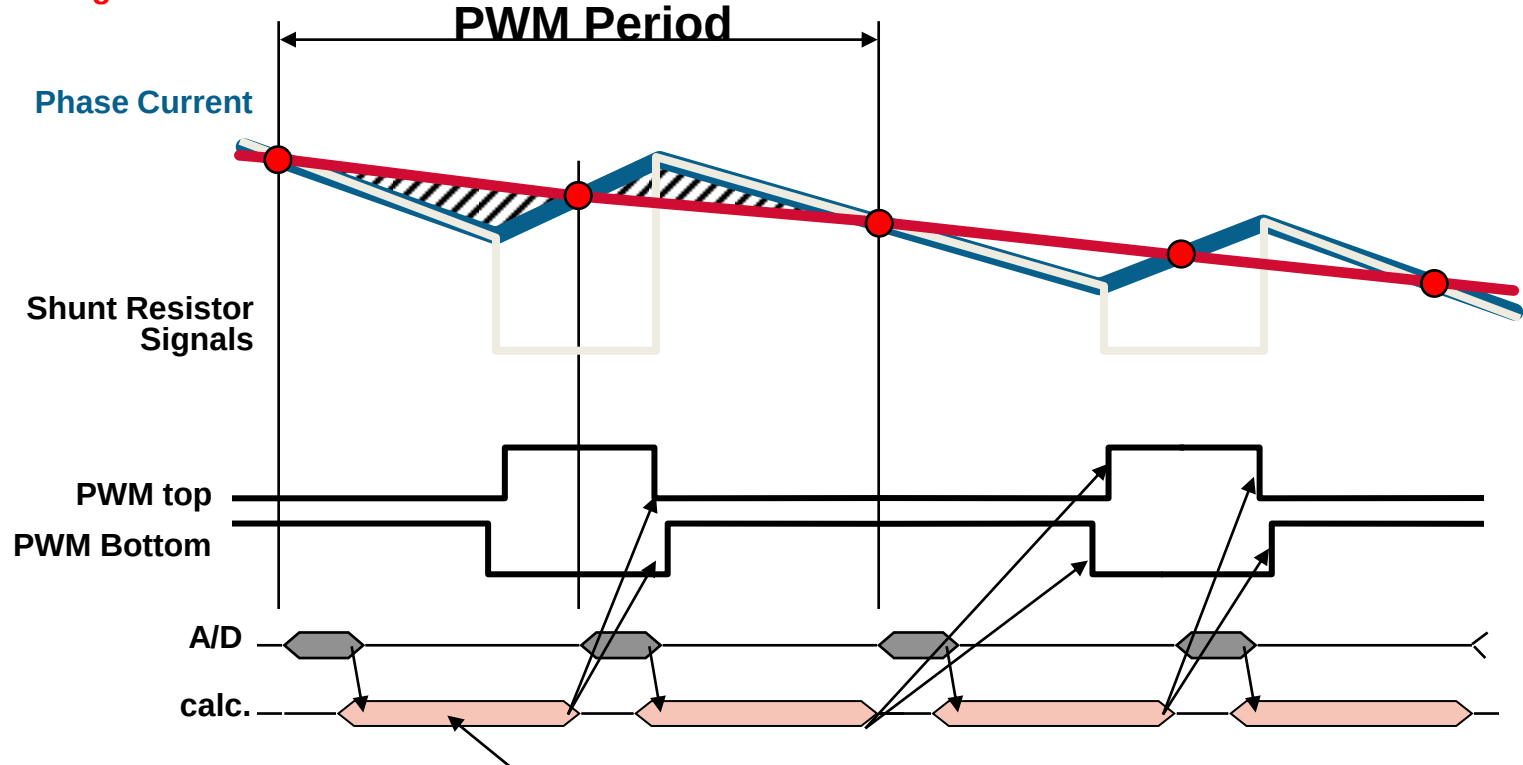
- PWM synchronization
 - Provide opportunity to
 - force FTM counter to its initial value (CNTINH:L) and the channel outputs are forced to initial value (known as FTM counter synchronization) and
 - update 3 kinds of registers (MOD, CnV, OUTMASK[CHnOM]) with their write buffers and sync two or more FTMs
 - Trigger event: hardware trigger or software trigger
 - Update point: boundary cycle
 - Minimum/low boundary (FTM counter == CNTINH:L)



FlexTimer

- PWM Synchronize with ADC
 - ADC sampling helps to filter the measured current – anti-aliasing
 - noise free sampling possible when the switch is inactive
 - Conversion at the point when the shunt resistor signal is available

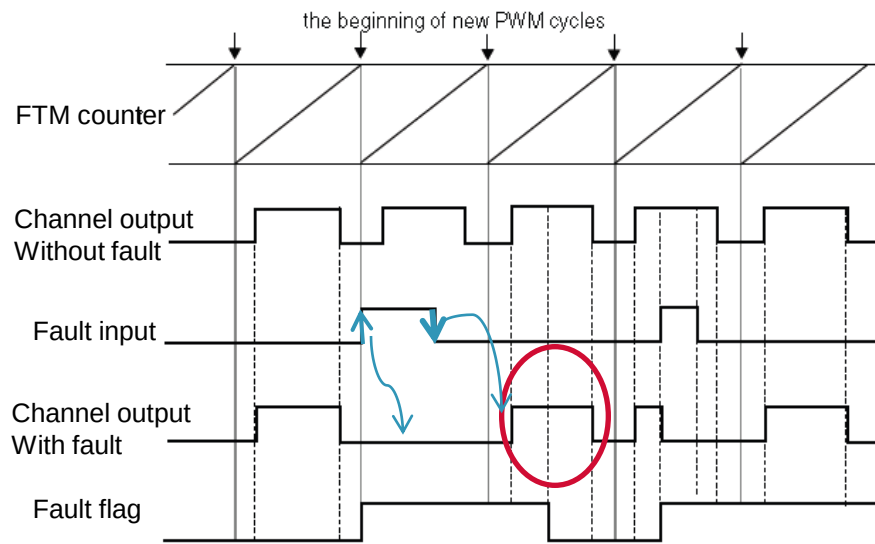
Sampling and Average Current



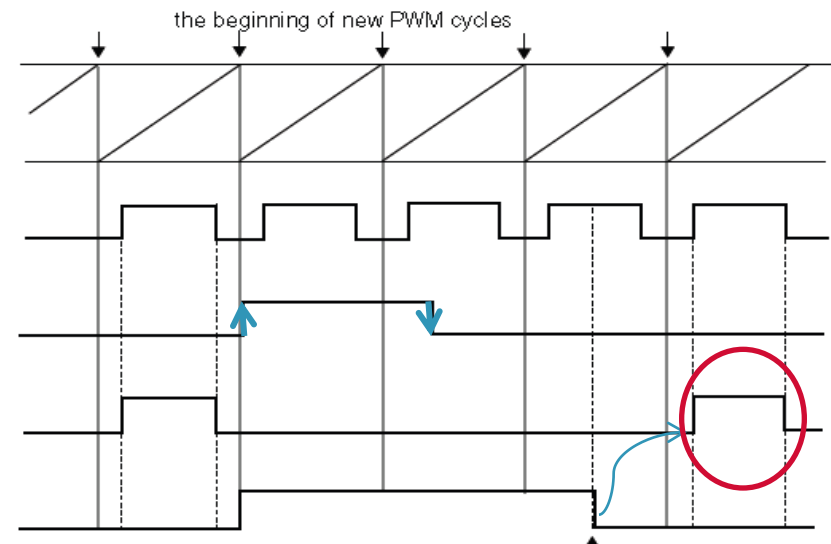
FlexTimer Fault Protection

- Channel outputs are forced to a safe value when a fault is detected
- Up to 4 fault control input pins with fault filters able to filter glitches of 15 system clocks wide
- Manual fault clearing (output re-enabled only when Fault flag cleared by s/w) and automatic fault clearing (output re-enabled when fault input returns to 0)

Automatic fault clearing

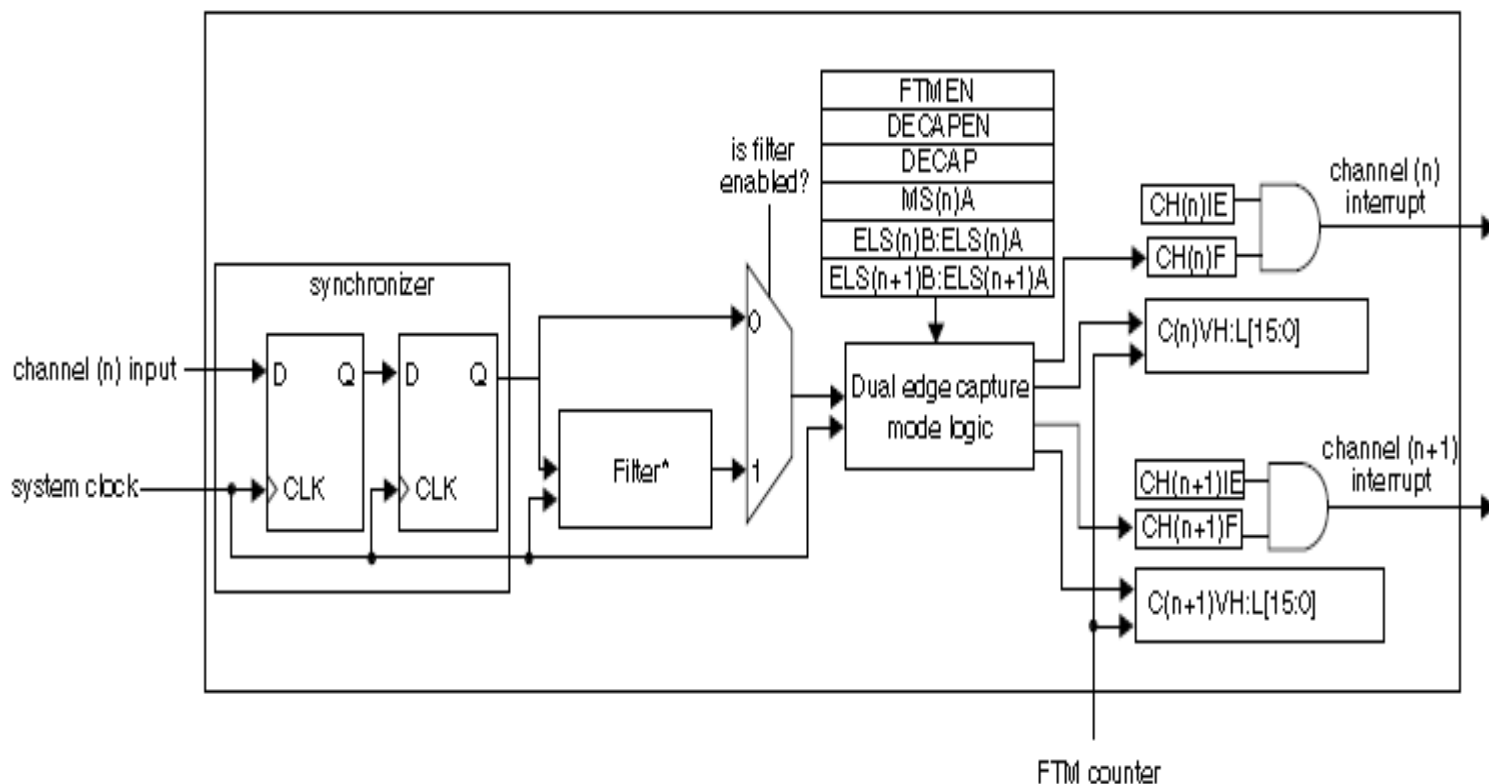


Manual fault clearing



FlexTimer Dual Edge Capture

- One-shot or continuous mode
- Pulse width measurement
- Period measurement



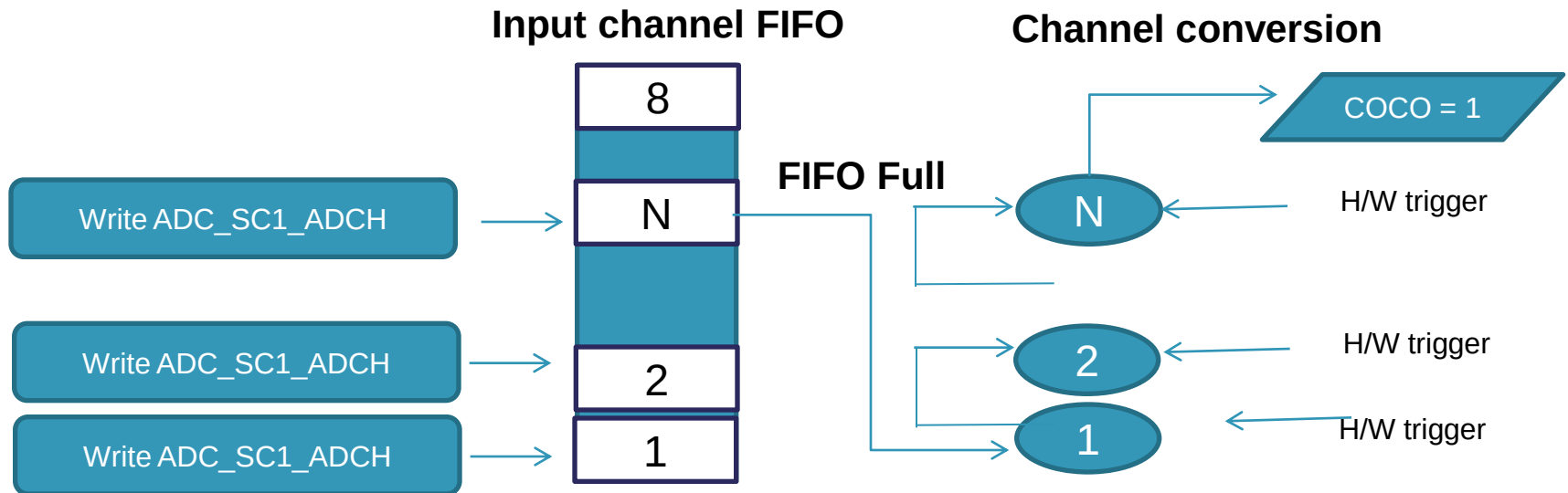
ADC with 8-entry FIFO

- Linear Successive Approximation algorithm with 8-, 10-, or 12-bit resolution
- Up to 16 external analog inputs, external pin inputs, and 5 internal analog inputs including internal bandgap, temperature sensor, and references
- Single or Continuous Conversion (automatic return to idle after single conversion)
- Operation in wait or stop3 modes for lower noise operation
- Automatic compare with interrupt for less-than, or greater-than or equal-to programmable value
- 8-entry channel FIFO and result FIFO to minimize the CPU overhead
 - Configurable FIFO depth from 2 to 8 entries as FIFO full condition
 - When channel FIFO is full:
 - For software trigger mode
 - Immediately start the first channel conversion, after the previous conversion completes, start the next conversion until the conversion of the last channel in FIFO depth completed, set conversion complete COCO flag
 - For hardware trigger mode
 - When the first trigger occurs, start the first conversion, after previous conversion completes and when the next trigger occurs, start the next conversion until all channels in FIFO depth completes conversion, then set conversion complete COCO flag

ADC with 8-entry FIFO

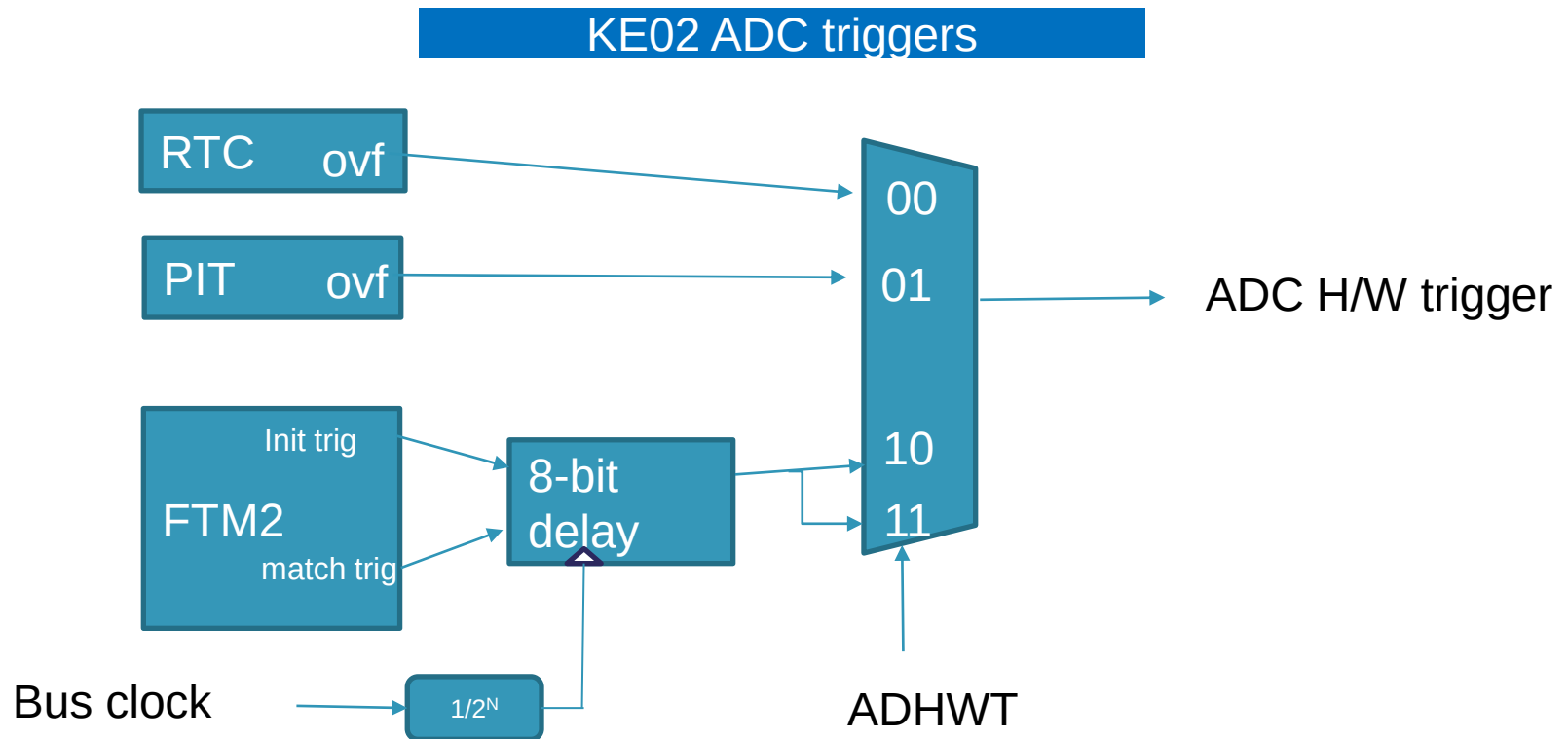
FIFO scan mode

- Always use the first dummied channel in spite of the value in the input channel FIFO to simplify the dummy work of input channel FIFO
- ADC conversion start to work in FIFO mode as soon as the first channel is dummied; when the previous conversion is completed, start the next conversion until the result FIFO is full and then set conversion complete COCO flag
- In continuous conversion in which the ADC_SC1[ADCO] bit is set, the ADC starts next round of conversion immediately when all conversions are completed.



ADC with FIFO

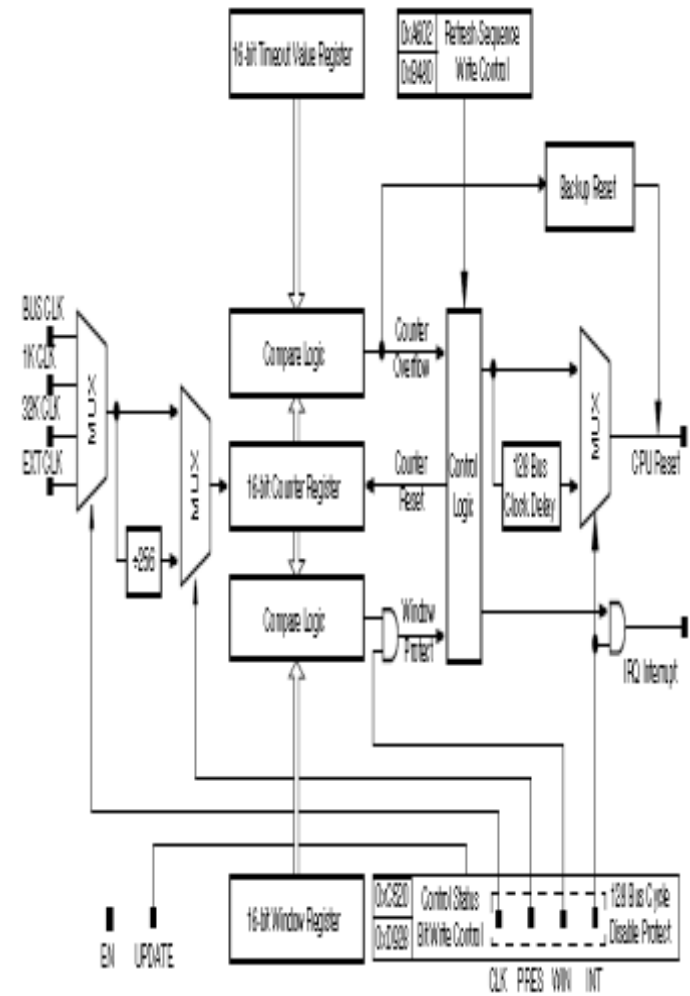
- ADC hardware trigger selection
 - RTC overflow/ PIT overflow/FTM2 trigger (match trigger or initialization trigger) with 8-bit programmable delay



NOTE: different devices may have different settings

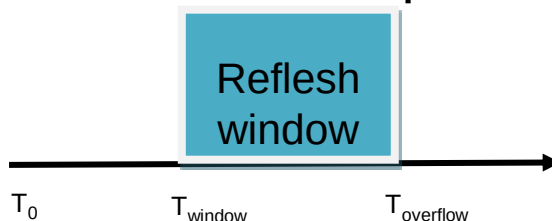
Watchdog (WDOG)

- Compliant with IEC60730 safety standard
- Independent clock source
 - Internal 32 kHz RC oscillator
 - internal 1 kHz RC oscillator
 - External clock
- 16-bit Programmable timeout period with optional fixed 256 clock prescaler when longer timeout periods are needed
- Robust write sequence for counter refresh
 - Refresh sequence of writing 0x02A6 and then 0x80B4 MUST be within 16 bus clocks



Watchdog (WDOG)

- Window mode option for the refresh mechanism
 - Programmable 16-bit window value
 - Provides robust check that program flow is faster than expected
 - Early refresh attempts trigger a reset
- Robust write sequence for unlocking write-once configuration bits
 - Configuration bits and registers are write-once-after-reset, to ensure watchdog configuration cannot be mistakenly altered
 - Unlock sequence of writing 0x20C5 and then 0x28D9 within 16 bus clocks for allowing updates to write-once configuration bits
- **Flexible test mode** enabling fast testing watchdog in the safety environment (either high 8-bit counter or lower 8-bit counter for comparison)
- **Backup reset** to prevent hardware lockup condition driven by bus clock

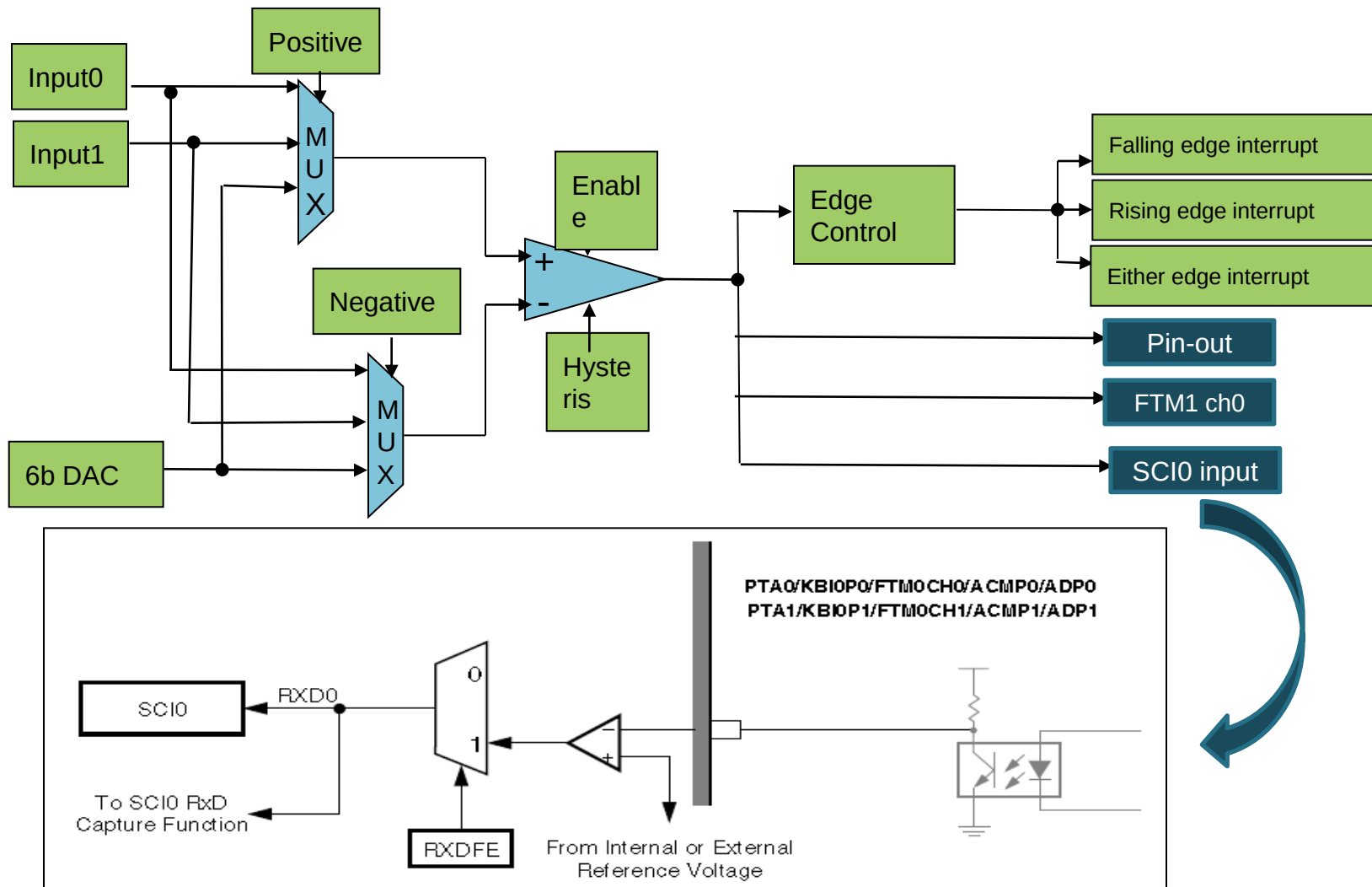


Cyclic Redundancy Check (CRC)

- 16/32-bit CRC code for error detection
- Programmable 16/32-bit initial seed value
- Programmable 16/32-bit polynomial
- Reverse input and output data by bit in a byte (no byte reverse)
- Final complement output of result

Name	Poly	Seed	Final XOR ?	Type of Transpose for Input	Type of Transpose for CRC Read	Standards
CRC-16	0x1021	0xFFFF (ITU-T V.41) 0x0000 (ITU-T T.30, X.25)	No	No transpose	No transpose	CRC-CCITT, ADCCP, SDLC/HDL C
CRC-16	0x1021	0	No	Transpose only bits in a byte	Transpose only bits in a byte	CRC-CCITT (Kermit)
XMODEM	0x8408	0x0000	No	Transpose only bits in a byte	Transpose only bits in a byte	XMODEM
ARC	0x8005	0x0000	No	Transpose only bits in a byte	Transpose only bits in a byte	ARC (zip file)
CRC-32	0x04C11DB7	0xFFFF FFFF	Yes	Transpose only bits in a byte	Transpose both bits and bytes	PKZIP, AUTODIN II, Ethernet, FDDI

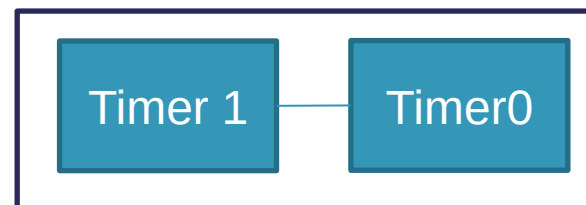
Analog Comparator (ACMP)



Periodic Interrupt Timer(PIT)

- An array of 32-bit count-down-to-0 timers that can be used to raise interrupts and triggers
- KE02 has two timers in a PIT
- Each timer can work independently
- Two timer can be chained to form a 64-bit timer
- A timer can be programmed to function in debug mode

64-bit timer





EMC Design Guideline for KE0x Real Case EMC Performance with Microwave Oven

Background

- Internal evaluation on EMC performance in board level and system level.
- Identify device capability in real application environments.
- A simplify microwave oven reference design is developed as a test platform.
- Include all hardware, firmware and mechanical design to provide a stable, controllable and precise environment for EMC measurement.

Test Platform

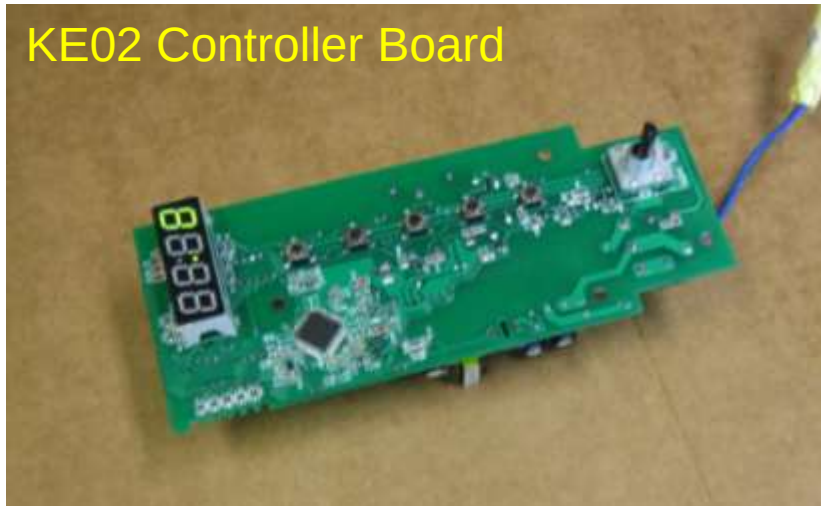
Application: Home Appliance

Product: Microwave oven

MCU: MKE02Z64VLD2 (64-LQFP)

Board: KE02 Controller Board with Power Supply

KE02 Controller Board



Microwave Oven



Test Results

Board level:

- *IEC 61000-4-4(EFT): +/- 4.4kV**
- *IEC 61000-4-2(ESD): Indirect Contact Discharge +/- 20kV*
- *China Appliance local test on AC Power Relay: 6-turns without Reset*

System level

- *IEC 61000-4-4(EFT): +/- 4.4kV**
- *IEC 61000-4-2(ESD): Contact Discharge (at the case) +/- 20kV*
- *IEC 61000-4-2(ESD): Air-Discharge (at the control panel) +/- 15kV*

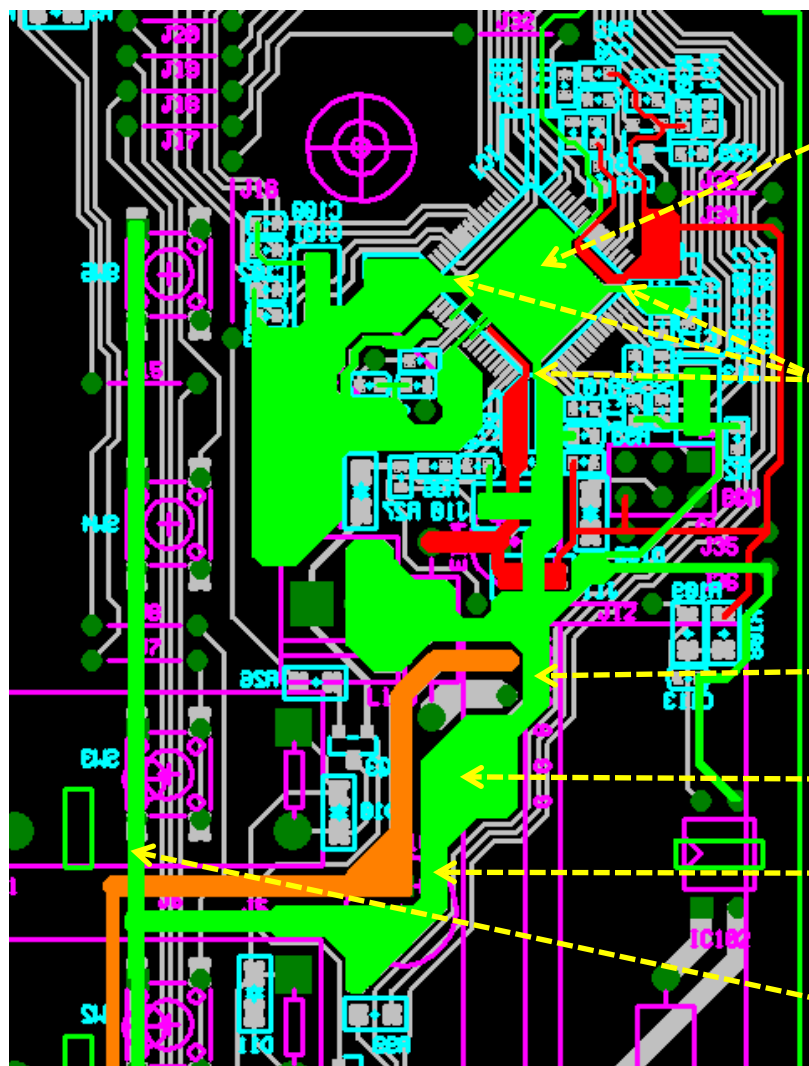
*Limited by the test equipment max output voltage

PCB Layout Recommendation

Ground Plane Connection:

- Rotate the KE02 package 45 degree for more easy routing on I/O pins.
- Fill up a ground plane underneath the MCU and connect all VSS pins together to ensure all VSS pins are kept at same potential level.
- The MCU ground plane can be further extended to the package corner points to achieve short ground paths with minimum loop area for other peripheral components around the MCU.
- Use separated ground trace to avoid ESD discharge energy directly inject to MCU ground.

PCB Layout Example 1 (Refer to AN4779)



Fill up a ground plane underneath the MCU and connect all VSS pins together with same potential level

Minimize the ground loops by use of the corner points for peripheral components around the MCU

5V GND

Power supply GND

12V GND

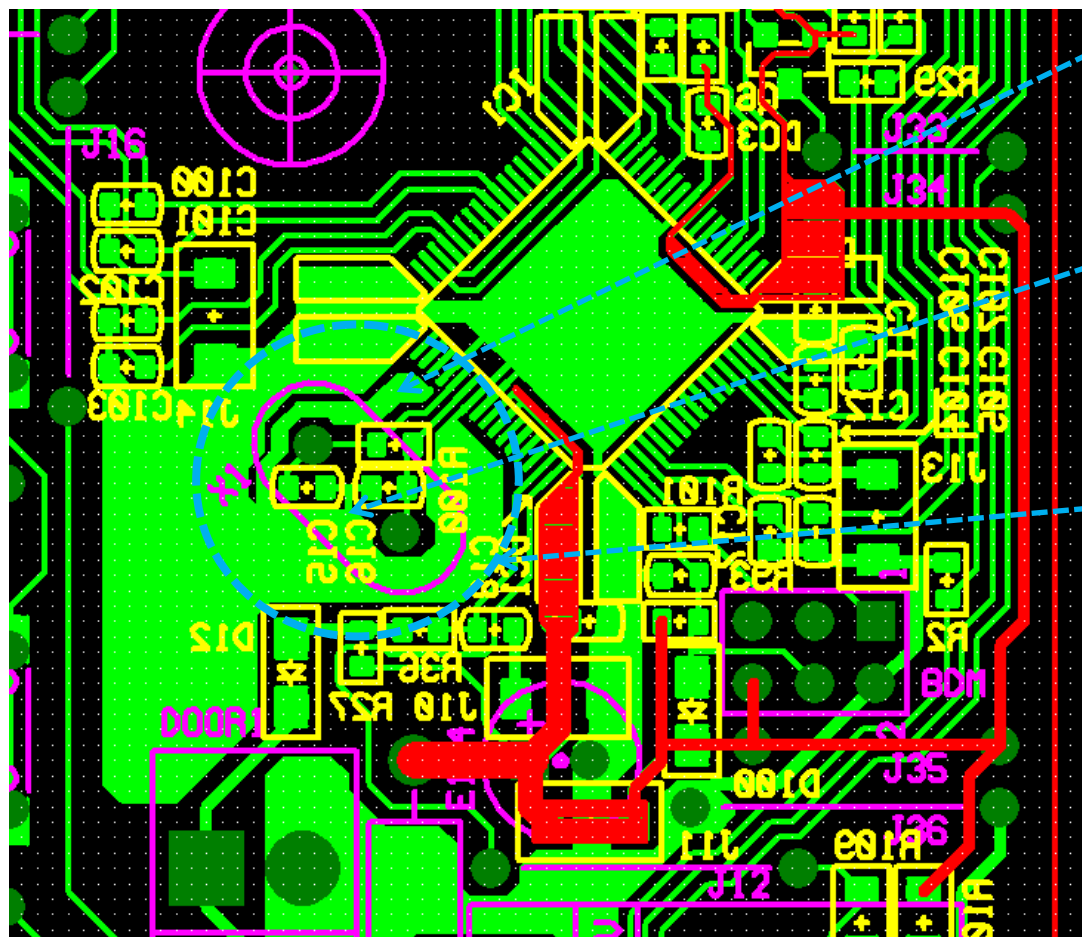
Avoid the ESD discharge energy injects into the 5V GND directly

PCB Layout Recommendation (cont.)

Crystal Oscillator Ground Connection:

- Place oscillator circuit components as close as possible to the XTAL and EXTAL pins.
- Do not place any signal trace near crystal circuit or across the bottom side of the circuit.
- Connect crystal oscillator load capacitors ground to the common ground plane.
- Route ground traces in the form of a guard ring, along with the traces connecting to the EXTAL and XTAL pins can minimize the noise coupling into the crystal circuit.

PCB Layout Example 2 (Refer to AN4779)



Add a guard ring (a ground trace with no current flow)

Connect crystal loading capacitors to a common ground plane

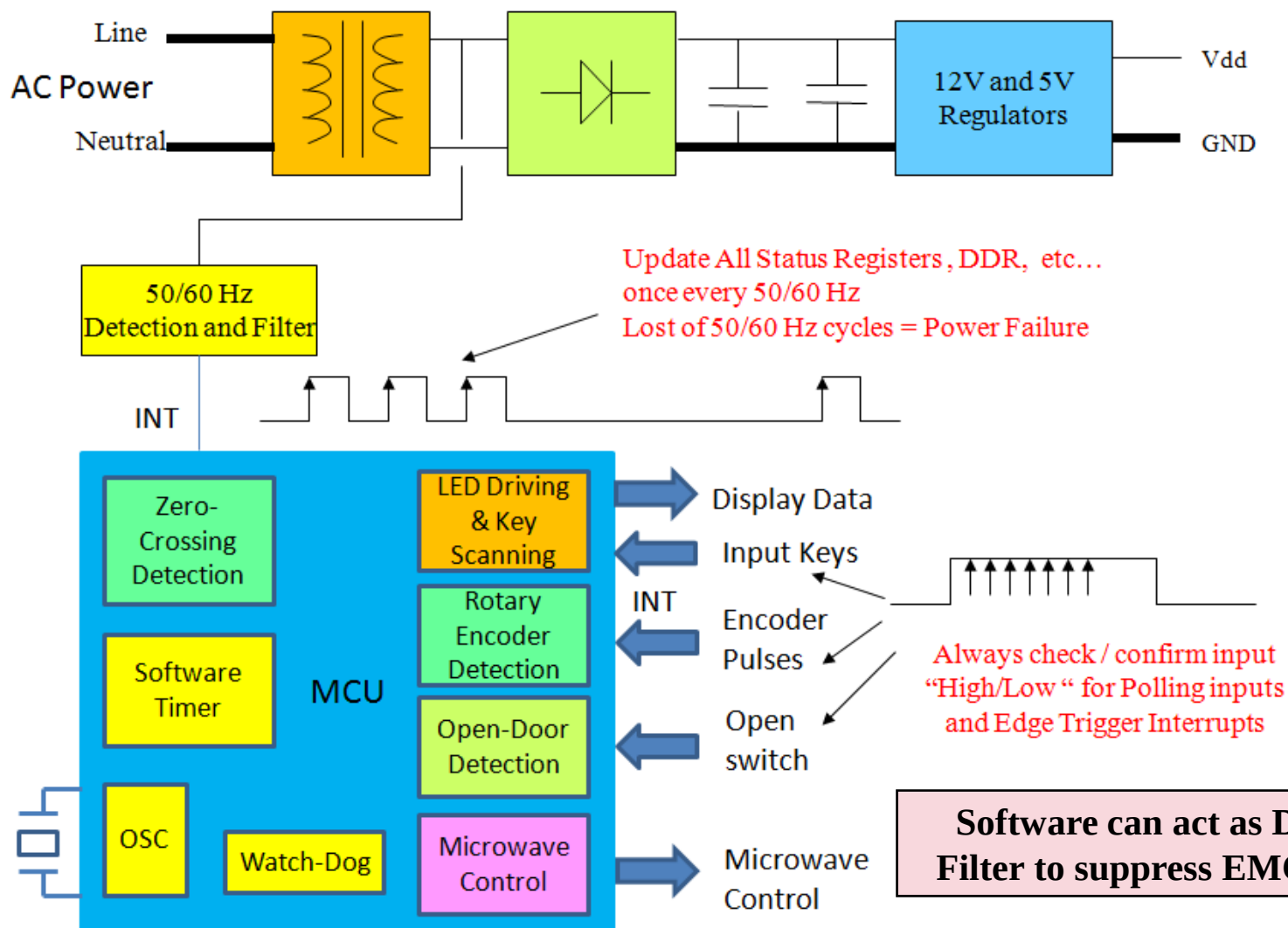
Avoid any signal trace near the oscillator circuit or across the bottom side of the circuit

Place the oscillator circuit to the EXTAL and XTAL pins as close as possible

Defensive Software Design

- The software design cannot change the physical media which couples the noise into the system, or reduce the absolute magnitude of noise generated from external sources.
- The software must be able to identify a particular event if it is a false alarm triggered by noise sources or it is a normal driven event and then make a smart decision on corresponding actions.
- Good defensive software design is one of the key factors to improve overall performance, system protection and operating stability in noisy environments (e.g. EMC).

System Configuration



Implementations

- Enable Watch-Dog to avoid code runaway.
- Refresh data direction setting registers periodically.
- Fill unused memory to avoid code runaway.
- Define all interrupt vectors even those that are not used.
- Select Frequency Locked Loop (FLL) engaged mode.
- Always re-confirm edge triggered event.
- Enable digital filter on input port.

Application Note for EMC

- [AN4779](#)
 - EMC Design Tips for Kinetis E Family
- [AN4438](#)
 - EMC Design Considerations for MC9S08PT60
- [AN4476](#)
 - System Design Guideline for 5V 8-bit families in Home Appliance Applications
- [AN4463](#)
 - How To Develop a Robust Software in Noise Environment
- [AN2321](#)
 - Designing for Board Level Electromagnetic Compatibility
- [AN2321_GB](#)
 - Designing for Board Level Electromagnetic Compatibility (Chinese Version)
- [AN2764](#)
 - Improving the Transient Immunity Performance of Microcontroller-Based Applications
- [AN1050](#)
 - Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- [AN1259](#)
 - System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

Application Note for EMC

- **AN1263**
 - Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- **AN1705**
 - Noise Reduction Techniques for Microcontroller-Based Systems
- **AN2015**
 - Power-On, Clock Selection, and Noise Reduction Techniques for the Motorola MC68HC908GP32
- **AN1744**
 - Resetting Microcontrollers During Power Transitions
- **EB413**
 - Resetting MCUs
- **AN1783**
 - Determining MCU Oscillator Start-up Parameters
- **EB396**
 - Use of OSC2/XTAL as a Clock Output on Motorola Microcontrollers
- **AN1706**
 - Microcontroller Oscillator Circuit Design Considerations
- **EB398**
 - Techniques to Protect MCU Applications Against Malfunction Due to Code Run-Away



Freedom and KE0x Driver Lib

Kinetis E Series MCUs Entry-level Enablement

Hardware

New

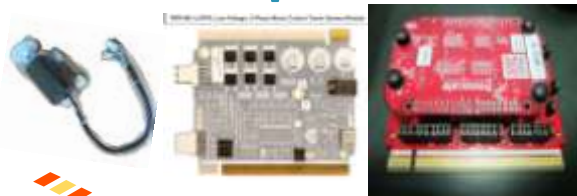
Freescal Freedom Development Platform

FRDM-KE02Z40M
FRDM-KE04Z
FRDM-KE06Z

- Low –cost platform for entry-level developers (**\$12.95 USD**)
- Features the Freescale open standard embedded serial and debug adapter (OpenSDA).



Arduino™
Compatible



IDE & Code Generation

Freescal & 3rd party IDEs

- Freescale CodeWarrior IDE v10.5: **free** 64KB
- Keil MDK: free 32KB
- IAR EWARM: free 32KB
- Atollic TrueStudio: free 8KB
- GCC ARM Embedded via Launchpad.net

Freescal Processor Expert Code Generator

- **Free** software generation tool for device drivers / start-up code
- 7 steps from project creation to debug – dramatically reduces development time
- Available within CodeWarrior IDE or as a standalone plug-in for IAR/Keil/GNU IDEs

CodeWarrior

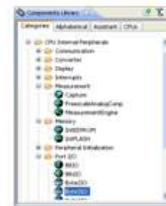


Rowley



GNU

atollic



Product Selection

Solution Advisor

www.freescale.com/sa

- Web-based interactive MCU selector
- Filters for operating characteristics, packaging, memory configuration & peripherals. Verifies muxing compatibility
- Save, download and print summary reports and pin mixing configurations



Kinetis E: HARDWARE Development Platforms

www.freescale.com/FRDM-KE02Z

Freedom Platform (FRDM-KE02Z)

The Freescale Freedom development platform is a set of software and hardware tools for evaluation and development. It is ideal for rapid prototyping of microcontroller-based applications. The Freescale Freedom KE02Z hardware, FRDM-KE02Z, is a simple, yet sophisticated design featuring a Kinetis E Series microcontroller, the industry's 5V microcontroller built on the ARM® Cortex™-M0+ core.

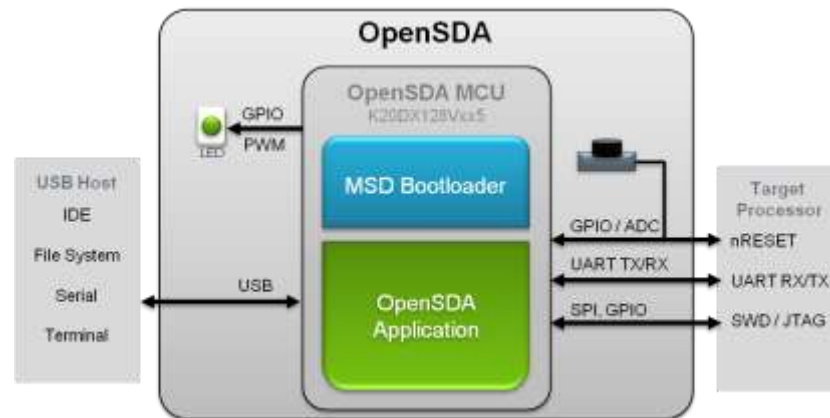
Features:

- MKE02Z64VQH2 MCU – 20MHz, 64KB Flash, 4KB SRAM, 64QFP
- Capacitive touch slider, MMA8451Q accelerometer, Tri-color LED
- Flexible power supply options – USB, external source
- Easy access to MCU I/O
- IrDA transmitter and receiver
- Thermistor sensor to measuring temperature
- Form factor compatible with Arduino™ R3 pin layout
- New, OpenSDA debug interface
 - Mass storage device flash programming interface (default)
 - no tool installation required to evaluate demo apps
 - P&E Debug interface provides run-control debugging and compatibility with IDE tools
 - CMSIS-DAP interface: new ARM standard for embedded debug interface

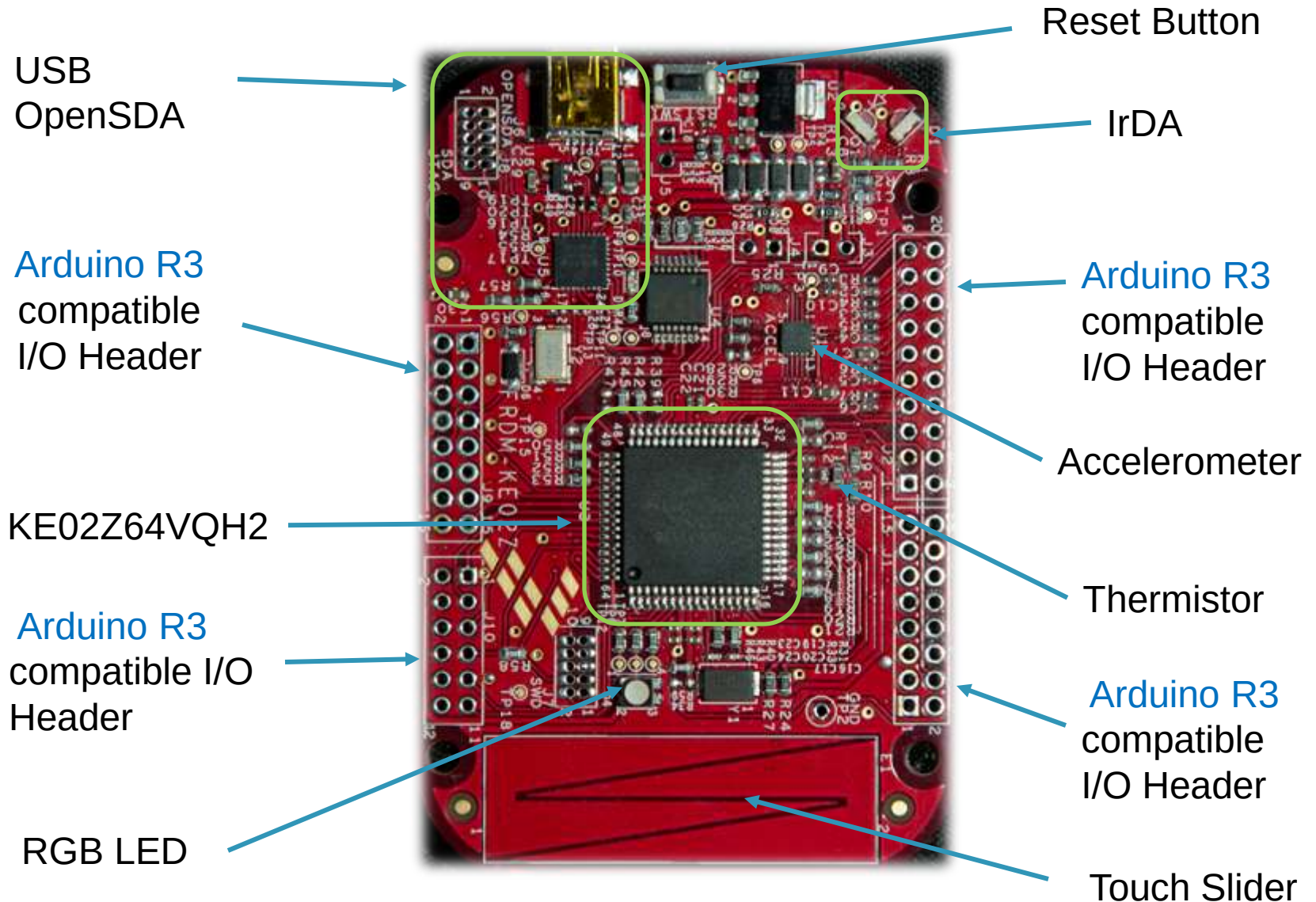
Refer to the *FRDM-KE02Z User's Manual* and *OpenSDA User's Guide* for more information.



Order Now
\$12.95

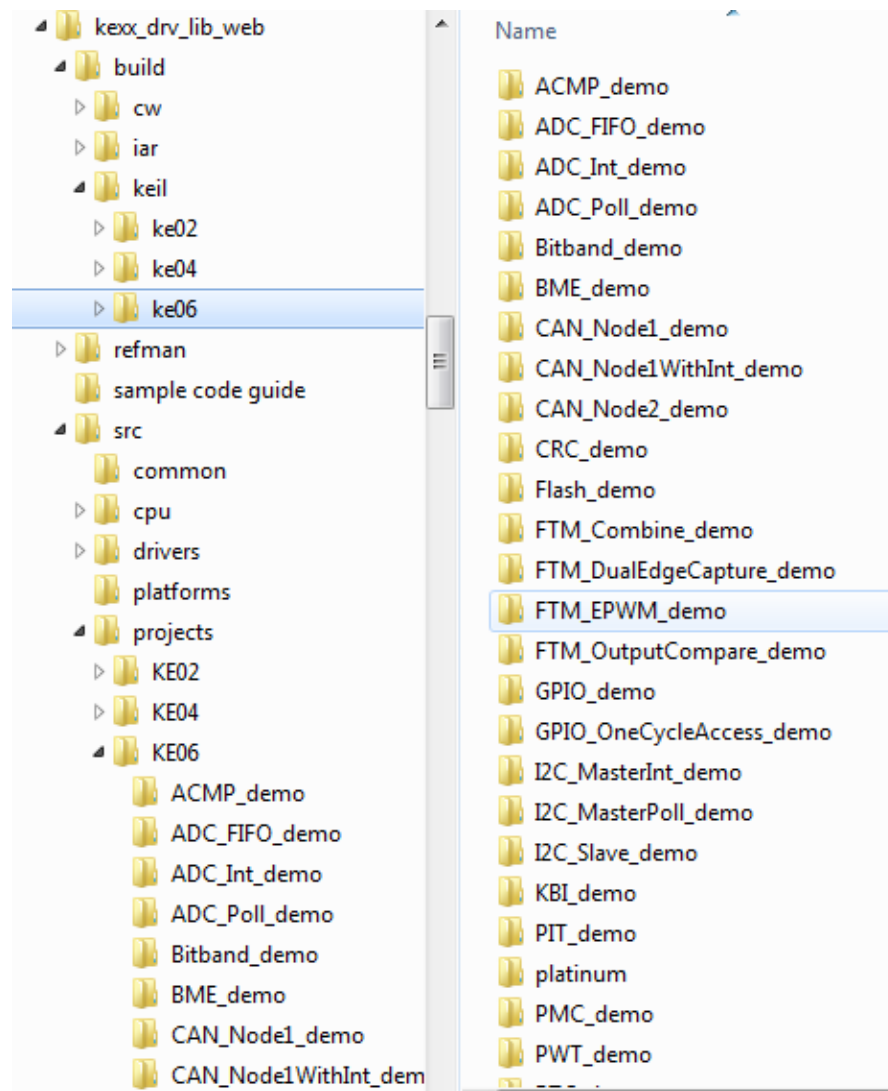


Get to know KE02 freedom



KE0x driver library

- **ARM CMSIS complaint coding format more friendly for ARM users**
- **Unified coding style for better readability, reusability, portability, and maintenance.**
- **Unified API easy to understand for other module developers**
- **More efficient code by using inline functions**
- **Cover all on-chip peripherals providing low level driver(register access) and high level driver**
- **Rich sample code for each module from simple to complicated**
- **API reference manual help user rapid to learn how to use it**



Demo

No	Labs
1	Lab demo for FAT and FCC – contain of IrDA, accelerometer, thermistor, SPI communication, RTC, slip touch down/up to switch demo.
2	Flash demo
3	Low Power demo
4	BLDC demo
5	RTC – calendar with triggering other modules
6	SPI - communication
7	Touch sensing with TSS lib demo
8	UART with interrupt demo
9	Fast GPIO demo
10	Flextimer demo
11	PIT demo
12	ADC FIFO
13	ACMP with trigger and interrupt
14	CRC demo

Summary

- Presented general Kinetis E overview
- Deep dive the key features
- EMC design guideline
- Talked about freedom and KE0x peripheral driver
- Demo

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